

# X570 AORUS ELITE WIFI

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55	PM_1VSOC , PM_1V8 , PM_09SOCS5 , PM_CLDO12

2015.12.30~B.L

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Title

Size

Custom

Document Number

X570 AORUS ELITE WIFI

Date:

Tuesday, June 18, 2019

Rev

1.0

Sheet

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of

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COVER SHEET

A vertical line with two points labeled B and C. B is below C. An arrow points from B to C.

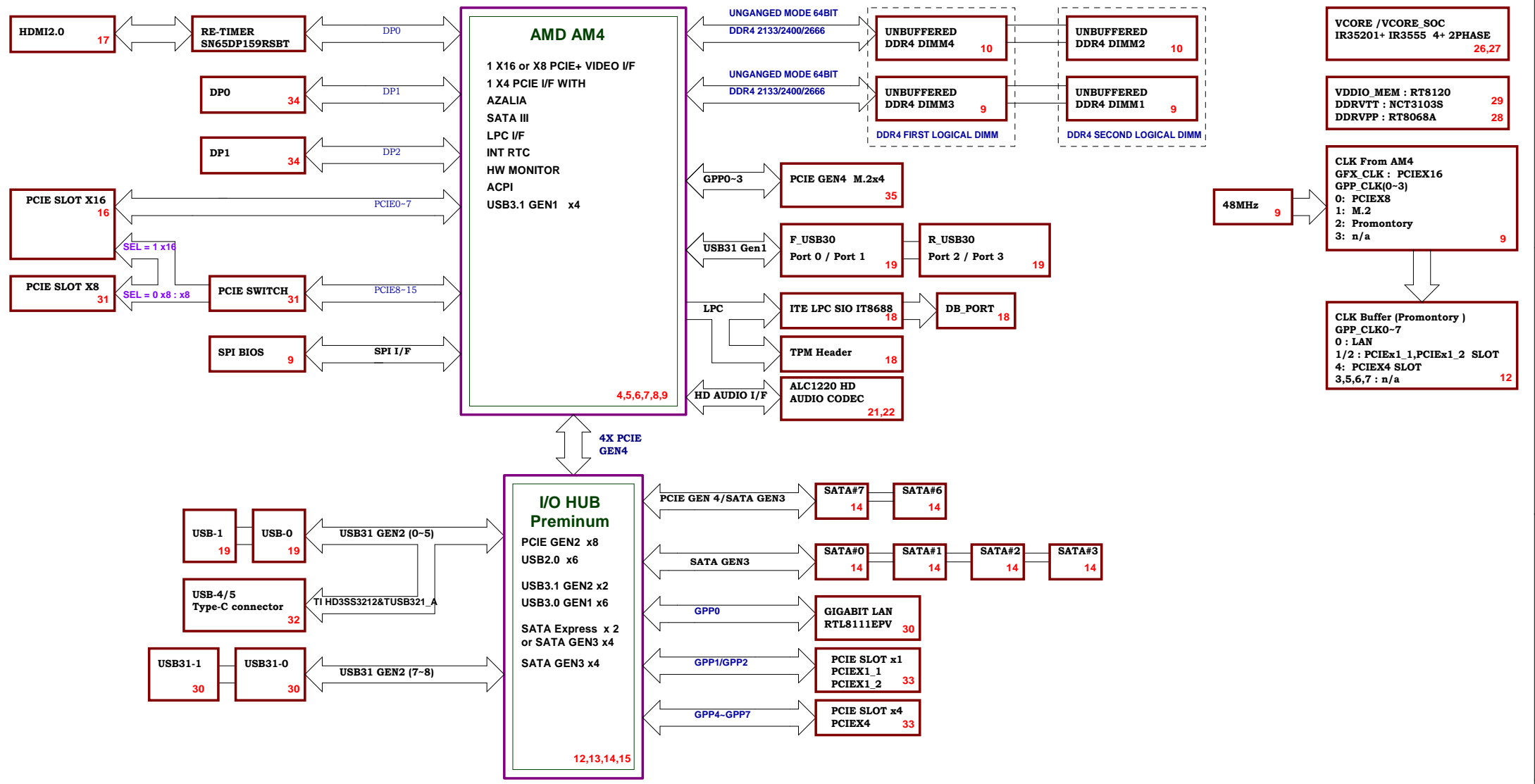
A

B

→

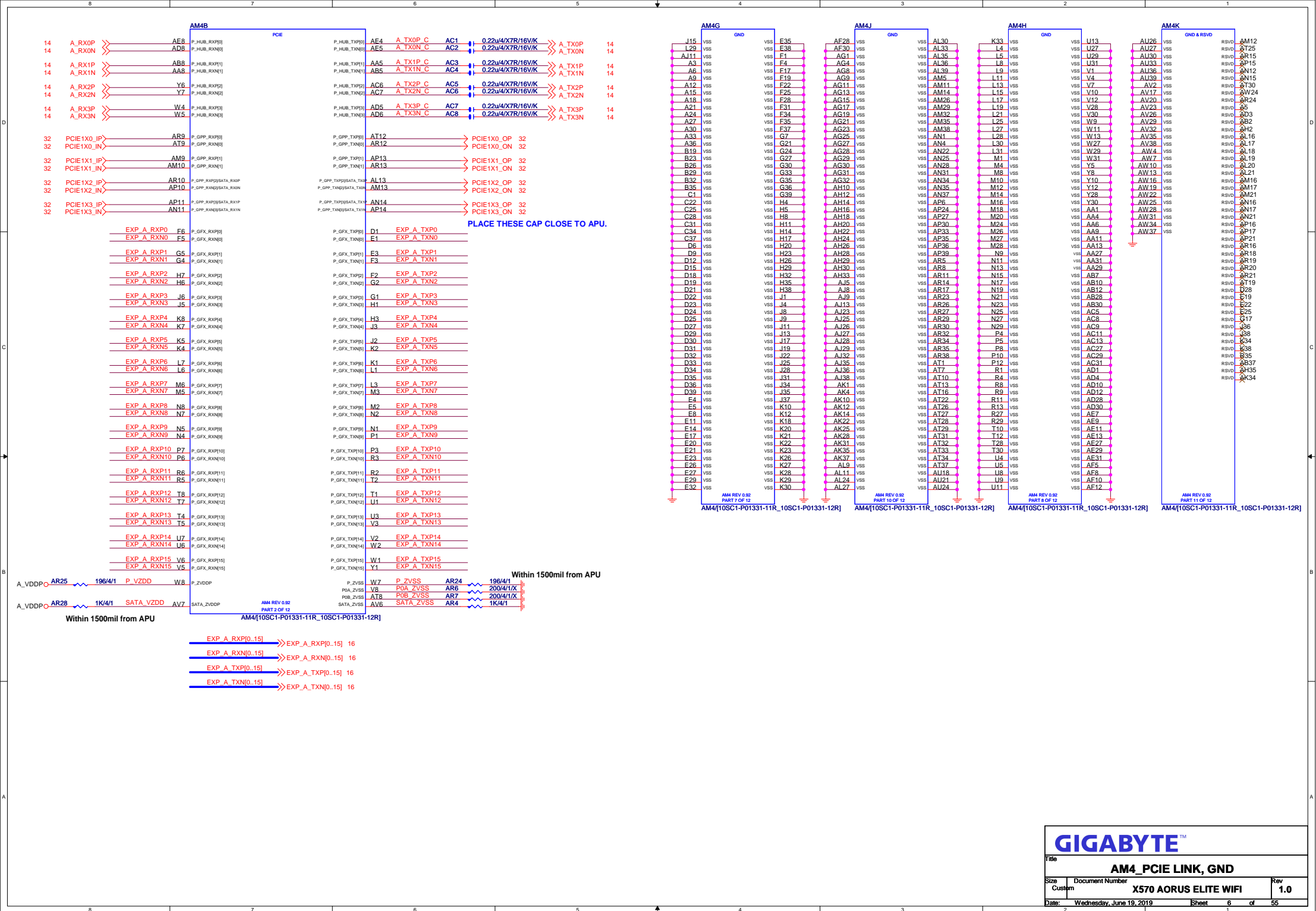
## 3

2





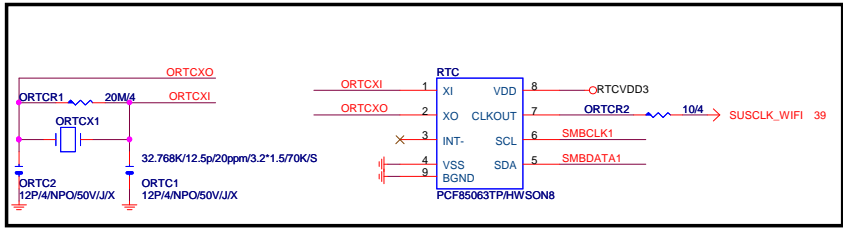
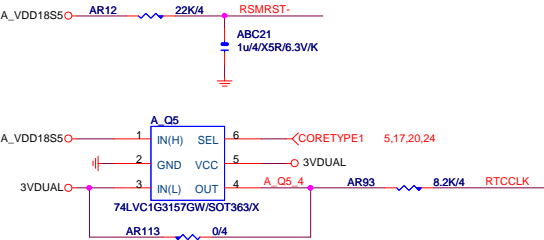




Internal Debug Only

TEST0	TEST1	TEST2	Description
0	0	0	FCH JTAG accessible from APU when TAPEN is asserted FCH JTAG pins overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserve
0	1	X	Reserve
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH JTAG can be accessed from FCH JTAG pins
1	TMS	1	Use on JTAG only, Yuba JTAG enable.

EC USB\_OC1  
NO TH  
NO MCU



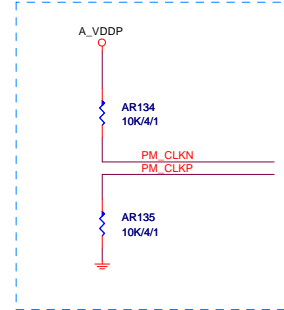
GIGABYTE™

AM4 MISC

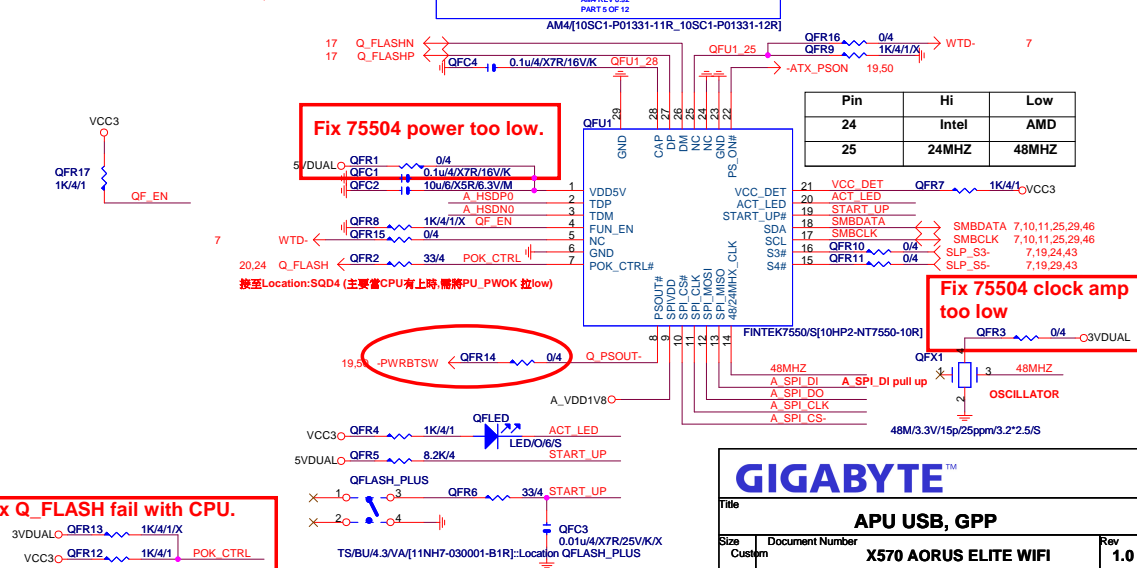
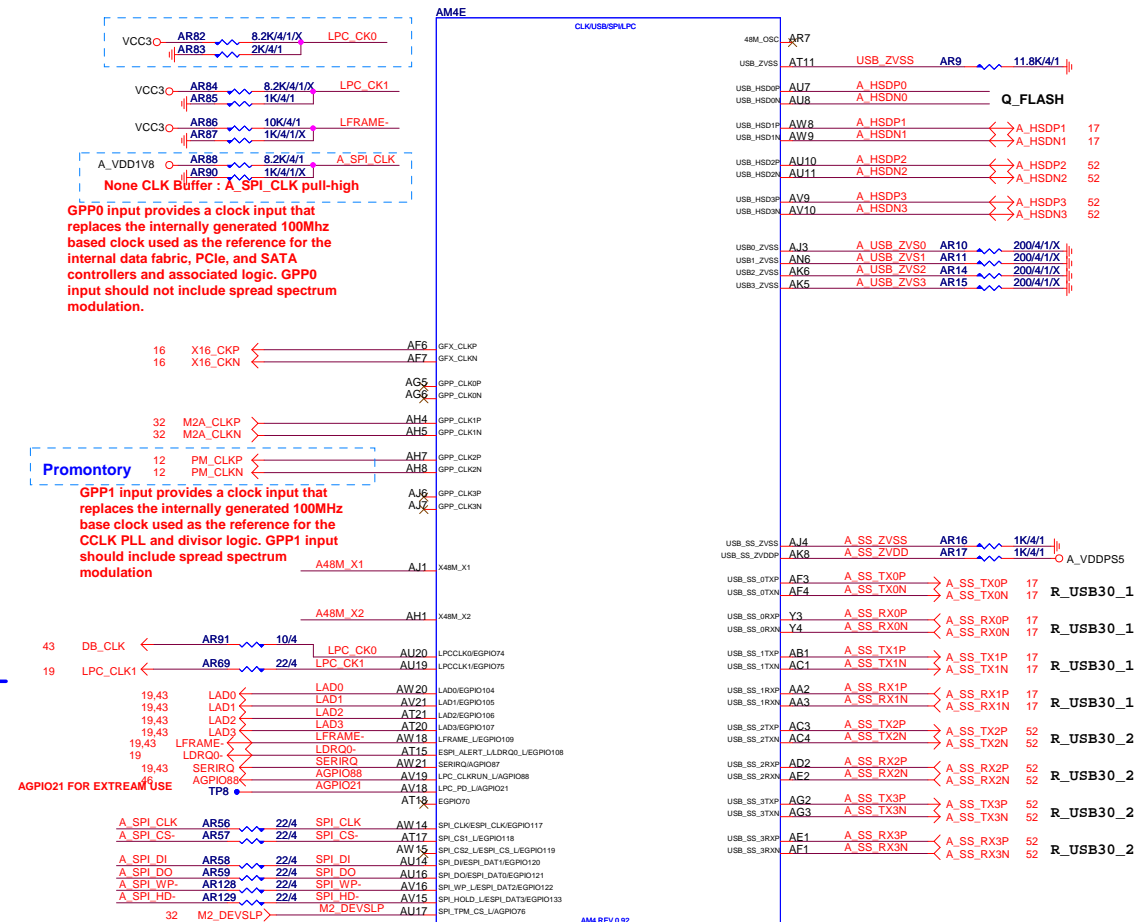
Size	Document Number	Rev
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19,43 LAD[0..3] << LAD[0..3]

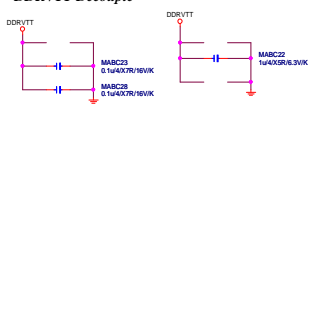
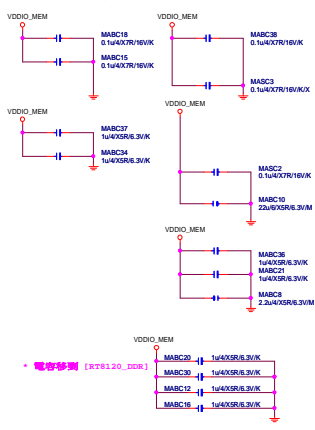
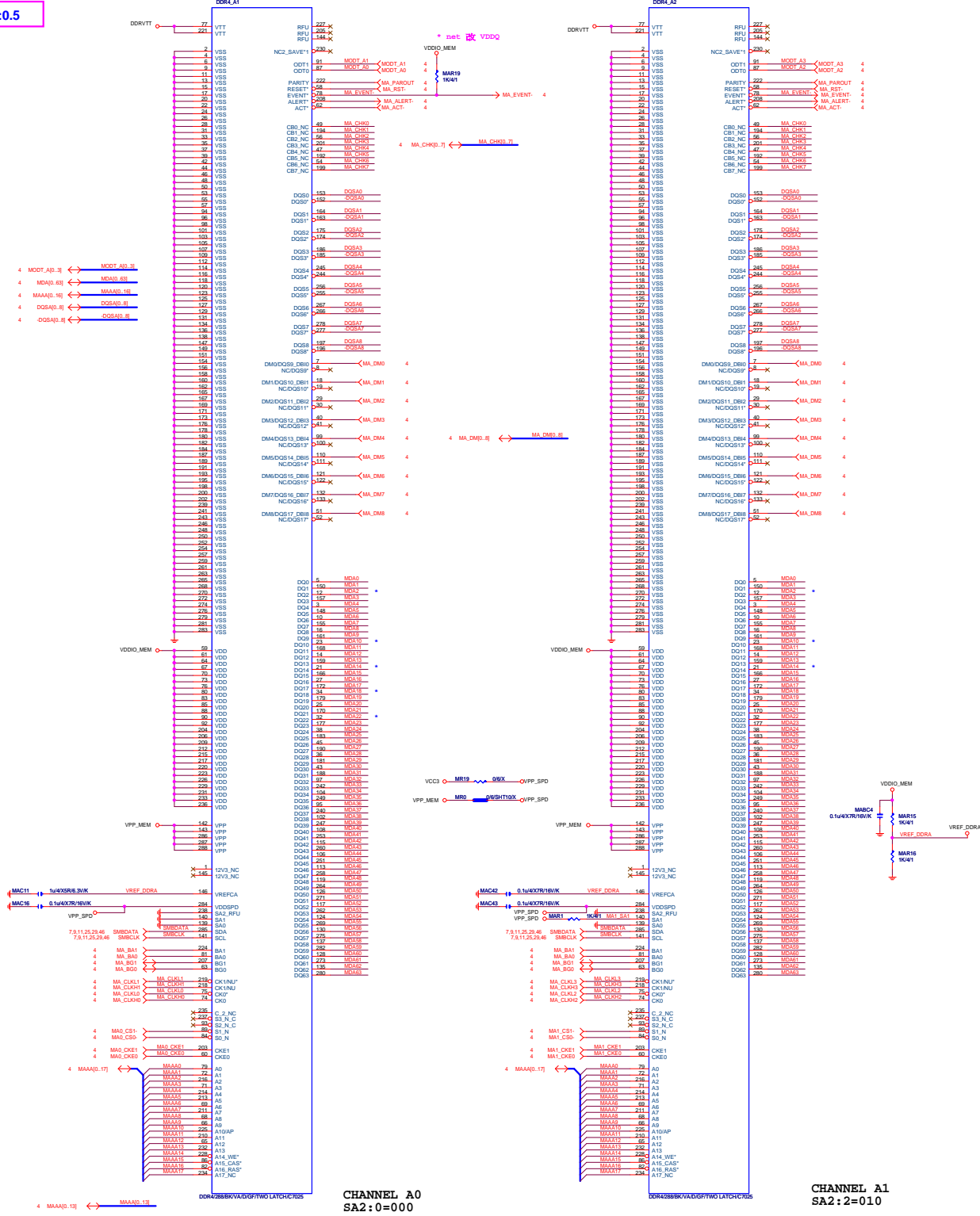


Pin	Hi	Low
24	Intel	AMD
25	24MHZ	48MHZ

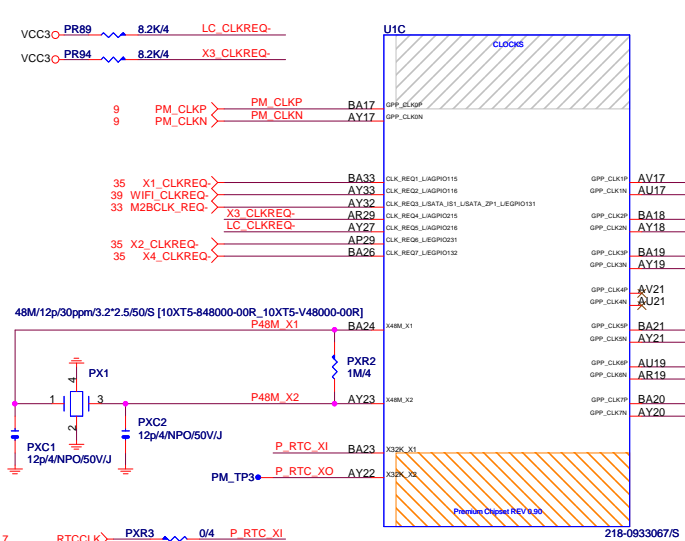
**Fix 75504 clock amp too low**

The diagram shows a resistor labeled QFR3 connected between a clock signal line (labeled 0/4) and a 3VDDUAL supply. The resistor is represented by a zigzag line.

			
Title			
APU USB, GPP			
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- AV17 GPP\_CLKP0 35
- AU17 GPP\_CLKN0 35
- BA18 CK\_WIFI\_100M\_DP 39
- AY18 CK\_WIFI\_100M\_DN 39
- BA19 M2B\_CLKP3 33
- AY19 M2B\_CLKN3 33
- AV21 LC\_SRCLK\_LAN 31
- AU21 LC\_SRCLK\_LAN 31
- BA21 GPP\_CLKP1 35
- AR19 GPP\_CLKN1 35
- BA20 X4\_CLKP 35
- AY20 X4\_CLKN 35

PCIEX1\_1 SLOT

WIFI

M.2B

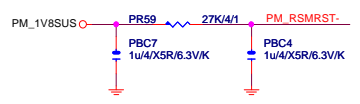
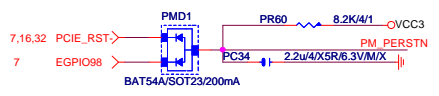
PCIEX1\_3 SLOT

1G LAN

PCIEX1\_2 SLOT

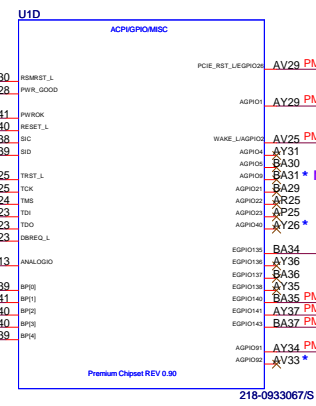
PCIEX X4 SLOT

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- PM\_RSMRST- AY30
- PM\_PWRGD BA28
- PM\_1V8O PR29 300/4
- PR19 4.7K/4/X
- PR20 4.7K/4/X
- PM\_1V8SUSO PR93 8.2K/4/1
- PR87 8.2K/4/1
- PR90 8.2K/4/1
- PR91 8.2K/4/1
- PR92 8.2K/4/1/X
- PM\_TP2 AP13
- PM\_1V8SUSO PR23 8.2K/4/X
- PR25 8.2K/4/X
- PR26 8.2K/4/X
- PR28 8.2K/4/X
- PR79 1K/4/1
- PM\_BP0 AW39
- PM\_BP1 AW41
- PM\_BP2 AW40
- PM\_BP3 AY40
- PM\_BP4 AY39

- APU\_SIC PR21 0/4
- APU\_SID PR22 0/4
- PM\_SIC
- PM\_SID

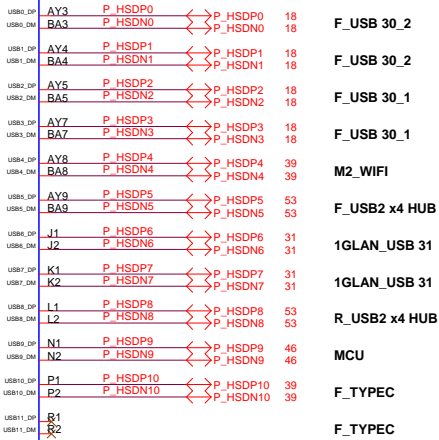
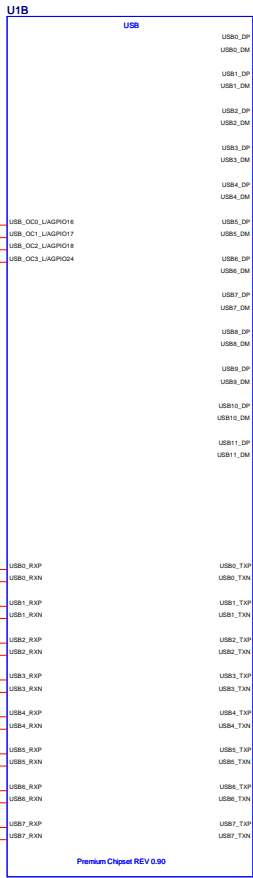


- AV29 PM\_RSTN PR1 22/4
- AY29 PM\_GPIO1 PR9 22/4/X
- AV25 PM\_PEWAKEN PR2 22/4
- BA31 \* NO CHARGE
- BA29
- BA25
- AP25
- AY26 \*
- BA34
- AY36
- BA36
- AY35
- BA35 PM\_EGPIOR140
- AY37 PM\_EGPIOR141
- BA37 PM\_EGPIOR143
- AY34 PM\_GPIO91
- AY33 \*

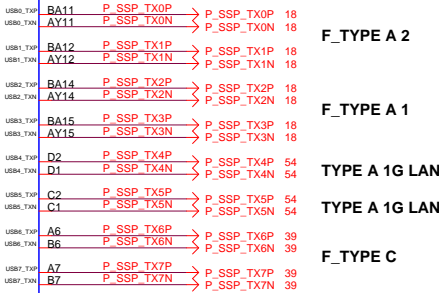
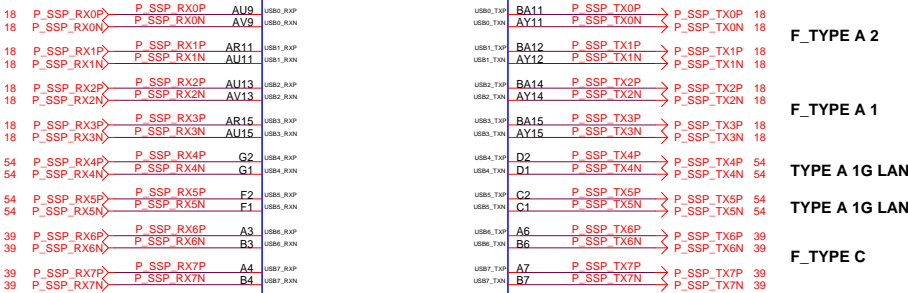
- PCIE\_WAKE- PR6 8.2K/4/X
- PM\_GPIO1 PR3 8.2K/4/X
- PM\_PEWAKEN PR2 22/4
- PM\_EGPIOR140 PR15 8.2K/4
- PM\_EGPIOR141 PR14 8.2K/4
- PM\_EGPIOR143 PR10 8.2K/4
- PM\_GPIO91 PR47 8.2K/4
- PM\_DBREQ- PR95 1K/4/1

PM\_GPIO11=>1: GPP clock output enabled,0: GPP clock output disabled

GIGABYTE		ANS 7128970	
Title			
PROMONTORY CPU/CLK/MISC			
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USB 3.1 Gen 2



USB Controller 0: USB20 [0:5], USB30 [0:3]

F\_TYPE A 1

TYPE A 1G LAN

USB Controller 1: USB20 [6:11], USB30 [4:7]

TYPE A 1G LAN

F\_TYPE C

USB Controller 0: USB20 [0:5], USB30 [0:3]

USB Controller 1: USB20 [6:11], USB30 [4:7]

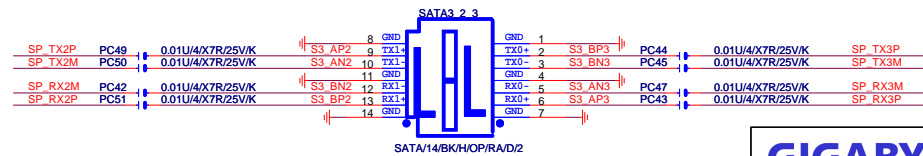
USB30G2	USB20
0	0
1	1
2	2
3	3
4	6
5	7
6	10
7	11

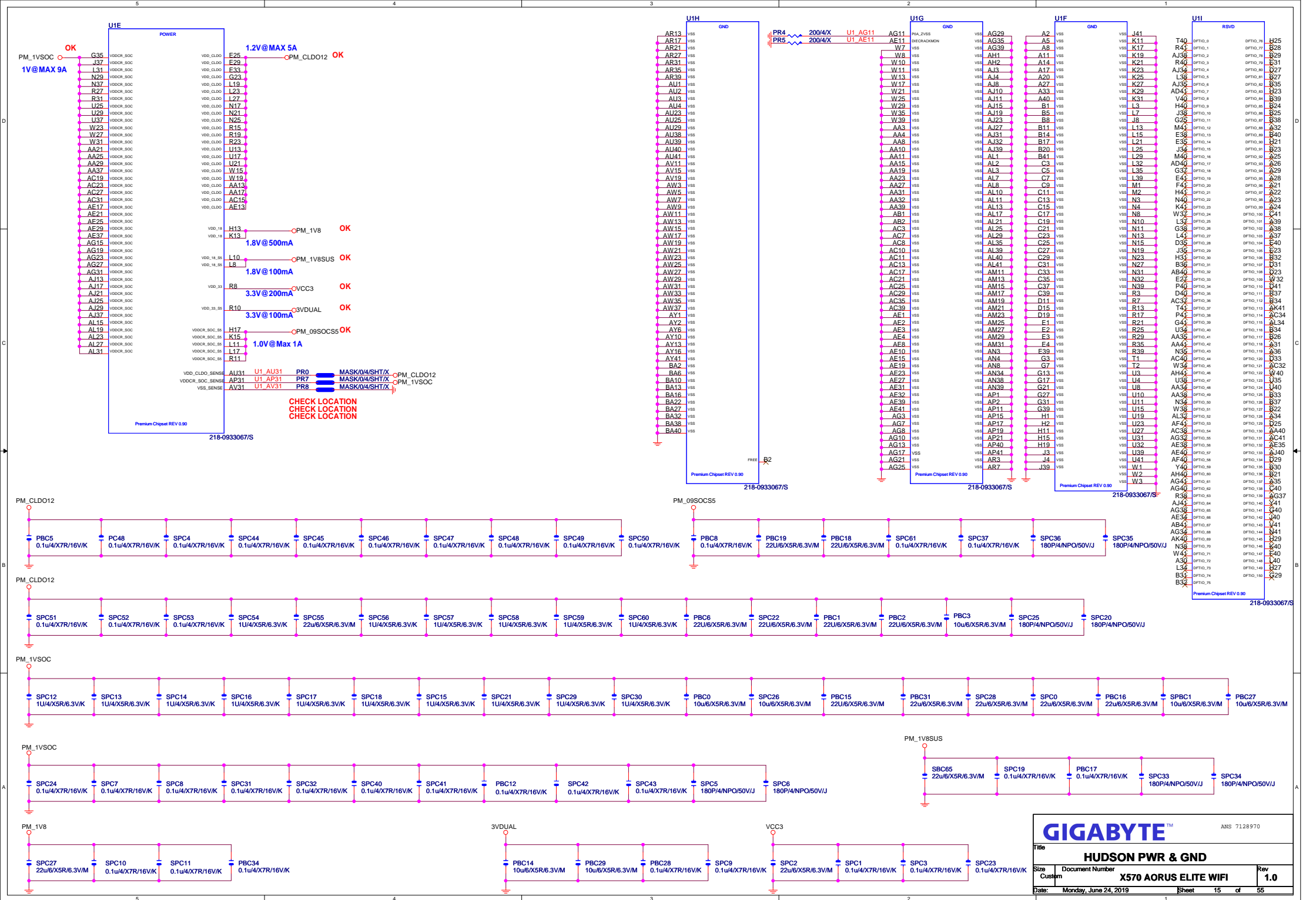
F\_USB 30\_2

F\_USB 30\_1

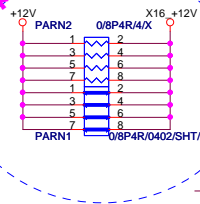
USB30\_I211 Lan

FRONT TYPE C





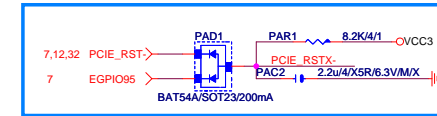
# +12 - protect short-wire test



0.22u/4/X5R/6.3V/K, Footprint: C0402-2

EXP A TXP0	PAC4	0.22u/4/X5R/6.3V/K	EXP A TXP0C
EXP A TXN0	PAC5	0.22u/4/X5R/6.3V/K	EXP A TXN0C
EXP A TXP1	PAC6	0.22u/4/X5R/6.3V/K	EXP A TXP1C
EXP A TXN1	PAC7	0.22u/4/X5R/6.3V/K	EXP A TXN1C
EXP A TXP2	PAC8	0.22u/4/X5R/6.3V/K	EXP A TXP2C
EXP A TXN2	PAC9	0.22u/4/X5R/6.3V/K	EXP A TXN2C
EXP A TXP3	PAC10	0.22u/4/X5R/6.3V/K	EXP A TXP3C
EXP A TXN3	PAC11	0.22u/4/X5R/6.3V/K	EXP A TXN3C
EXP A TXP4	PAC12	0.22u/4/X5R/6.3V/K	EXP A TXP4C
EXP A TXN4	PAC13	0.22u/4/X5R/6.3V/K	EXP A TXN4C
EXP A TXP5	PAC14	0.22u/4/X5R/6.3V/K	EXP A TXP5C
EXP A TXN5	PAC15	0.22u/4/X5R/6.3V/K	EXP A TXN5C
EXP A TXP6	PAC16	0.22u/4/X5R/6.3V/K	EXP A TXP6C
EXP A TXN6	PAC17	0.22u/4/X5R/6.3V/K	EXP A TXN6C
EXP A TXP7	PAC18	0.22u/4/X5R/6.3V/K	EXP A TXP7C
EXP A TXN7	PAC19	0.22u/4/X5R/6.3V/K	EXP A TXN7C
EXP A TXP8	PAC20	0.22u/4/X5R/6.3V/K	EXP A TXP8C
EXP A TXN8	PAC21	0.22u/4/X5R/6.3V/K	EXP A TXN8C
EXP A TXP9	PAC22	0.22u/4/X5R/6.3V/K	EXP A TXP9C
EXP A TXN9	PAC23	0.22u/4/X5R/6.3V/K	EXP A TXN9C
EXP A TXP10	PAC24	0.22u/4/X5R/6.3V/K	EXP A TXP10C
EXP A TXN10	PAC25	0.22u/4/X5R/6.3V/K	EXP A TXN10C
EXP A TXP11	PAC26	0.22u/4/X5R/6.3V/K	EXP A TXP11C
EXP A TXN11	PAC27	0.22u/4/X5R/6.3V/K	EXP A TXN11C
EXP A TXP12	PAC28	0.22u/4/X5R/6.3V/K	EXP A TXP12C
EXP A TXN12	PAC29	0.22u/4/X5R/6.3V/K	EXP A TXN12C
EXP A TXP13	PAC30	0.22u/4/X5R/6.3V/K	EXP A TXP13C
EXP A TXN13	PAC31	0.22u/4/X5R/6.3V/K	EXP A TXN13C
EXP A TXP14	PAC32	0.22u/4/X5R/6.3V/K	EXP A TXP14C
EXP A TXN14	PAC33	0.22u/4/X5R/6.3V/K	EXP A TXN14C
EXP A TXP15	PAC34	0.22u/4/X5R/6.3V/K	EXP A TXP15C
EXP A TXN15	PAC35	0.22u/4/X5R/6.3V/K	EXP A TXN15C

EXP A RXP0.15] >> EXP A RXP0.15] 6  
EXP A RXN0.15] >> EXP A RXN0.15] 6  
EXP A TXP0.15] >> EXP A TXP0.15] 6  
EXP A TXN0.15] >> EXP A TXN0.15] 6



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Title **PCI EXPRESS X 16**

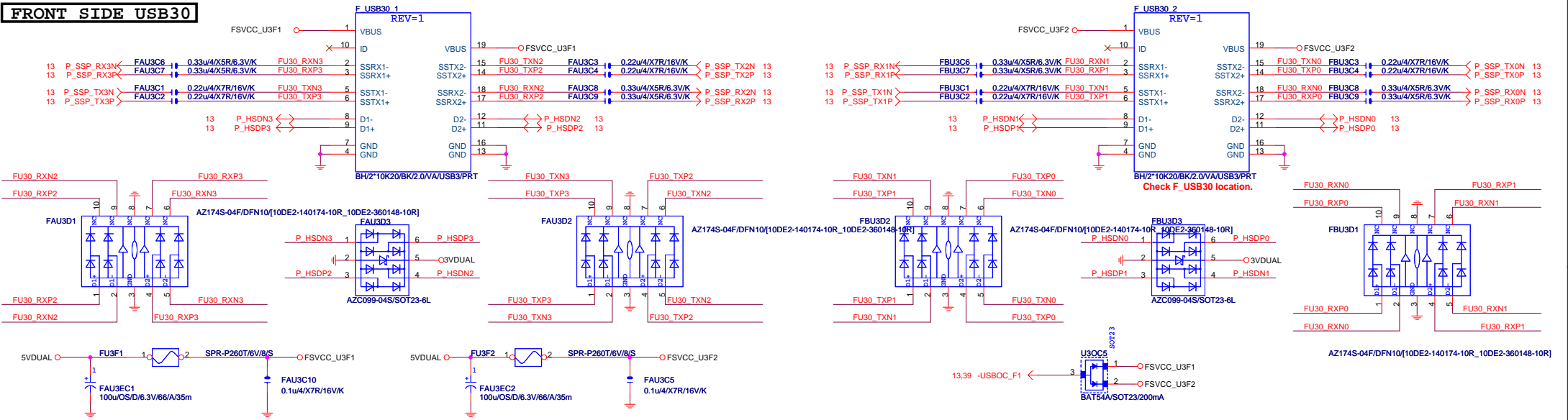
Size Custom Document Number **X570 AORUS ELITE WIFI** Rev **1.0**

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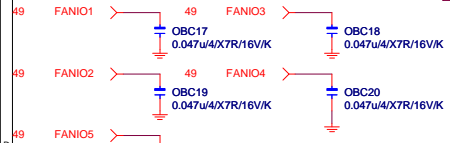


# FRONT SIDE USB30



# SIO IT8628CX REV:1.09

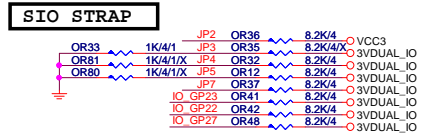
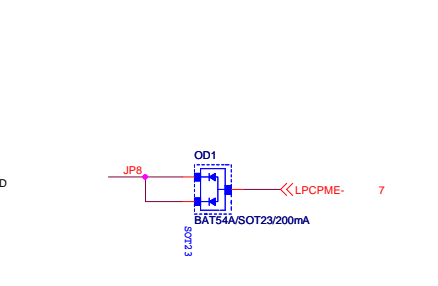
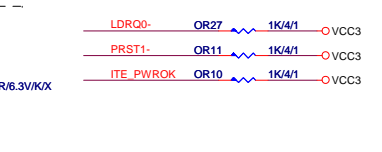
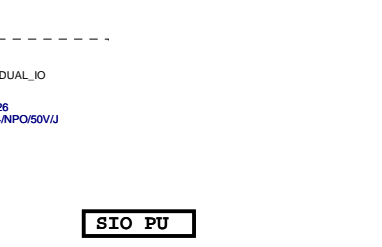
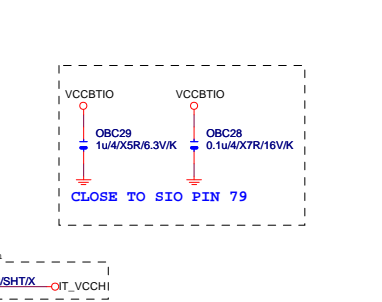
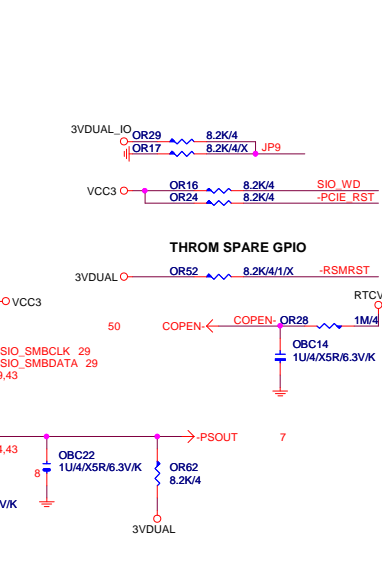
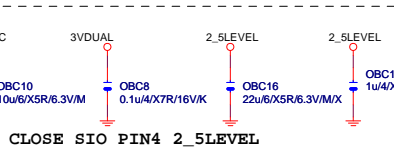
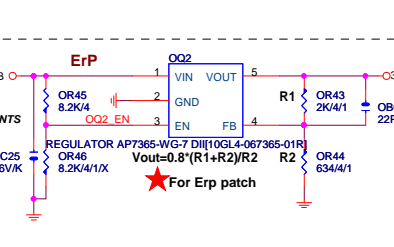
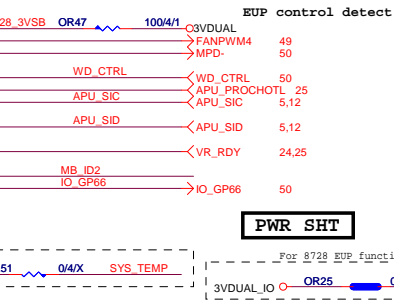
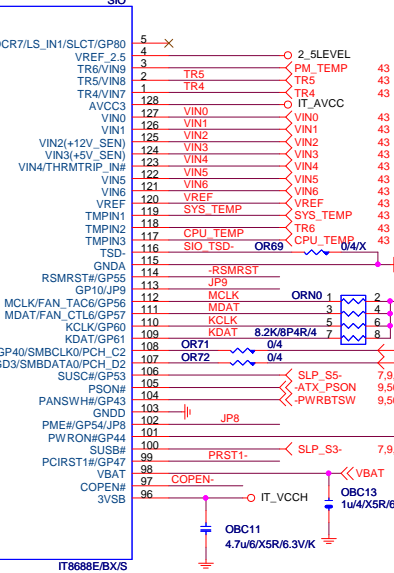
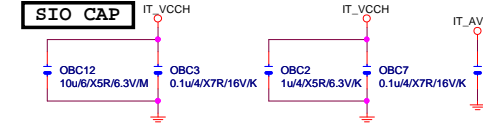
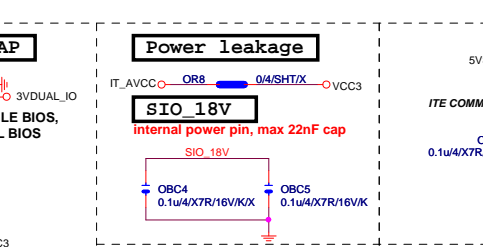
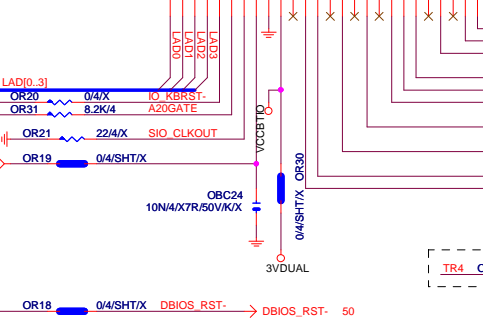
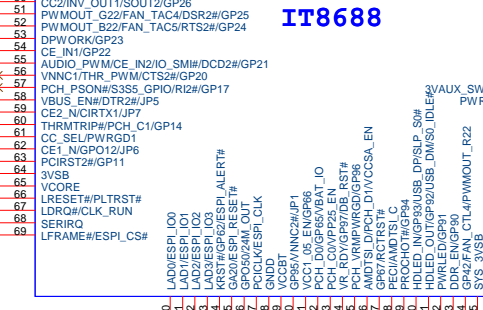
VCC3 0.047u/4X7R/16V/K  
OR38 8.2K/4X IO GP64  
OR39 8.2K/4X IO GP63  
OR40 8.2K/4X FAN\_ZERO



JP2  
JP3  
JP4  
FANPWM5



## IT8688



JP2	1	Disable WDT to rest PWROK
	0	Enable WDT to rest PWROK
JP3		Dual-BIOS CS pin mode select bit "0"
		See the below table
JP4	1	LPC/ESPI power VCCBT = 3.3V
	0	LPC/ESPI power VCCBT = 1.8V
JP5	1	LPC I/F
	0	ESPI I/F
JP6	1	Enable Dual BIOS Function (for GigaByte Only)
	0	Disable Dual BIOS Function (for GigaByte Only)
JP7		Dual-BIOS CE pin mode select bit "1"
		See the below table
	1 1	CE pin disable (Hold pin mode)
JP7	1 0	CE mode 1
JP3	0 1	CE mode 2
	0 0	CE mode 3

**GIGABYTE**

**ITE 8686 LPC IO, TPM, KB/MS**

Size

Document Number

Custom

X570 AORUS ELITE WIFI

Rev

1.0

Date

Wednesday, June 19, 2019

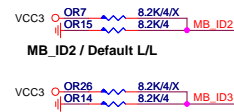
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## MB ID



FAN TABLE	
CPU_FAN	FAN_CTL1 FAN_TAC1
SYS_FAN1	FAN_CTL2 FAN_TAC2
SYS_FAN2	FAN_CTL3 FAN_TAC3
SYS_FAN3	FAN_CTL4 FAN_TAC4
OPT_FAN or SYS_FAN4	FAN_CTL5 FAN_TAC5
THRMTRIP	PIN56
PROCHOT	PIN89

## DUAL BIOS OPT STRAP

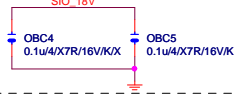
OR58 上件/OR56 不上件 SINGLE BIOS,  
OR58 不上件/OR56 上件 DUAL BIOS

## EMI

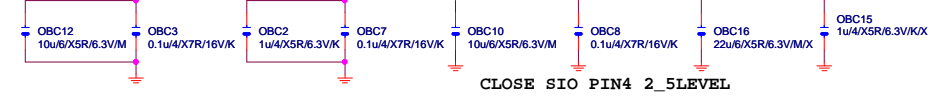


## Power leakage

IT\_AVCC - OR8 0.047u/4X7R/16V/K VCC3  
**SIO\_18V**  
internal power pin, max 22nF cap

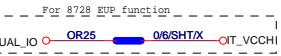


## SIO CAP

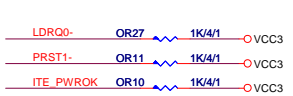


CLOSE SIO PIN4 2\_5LEVEL

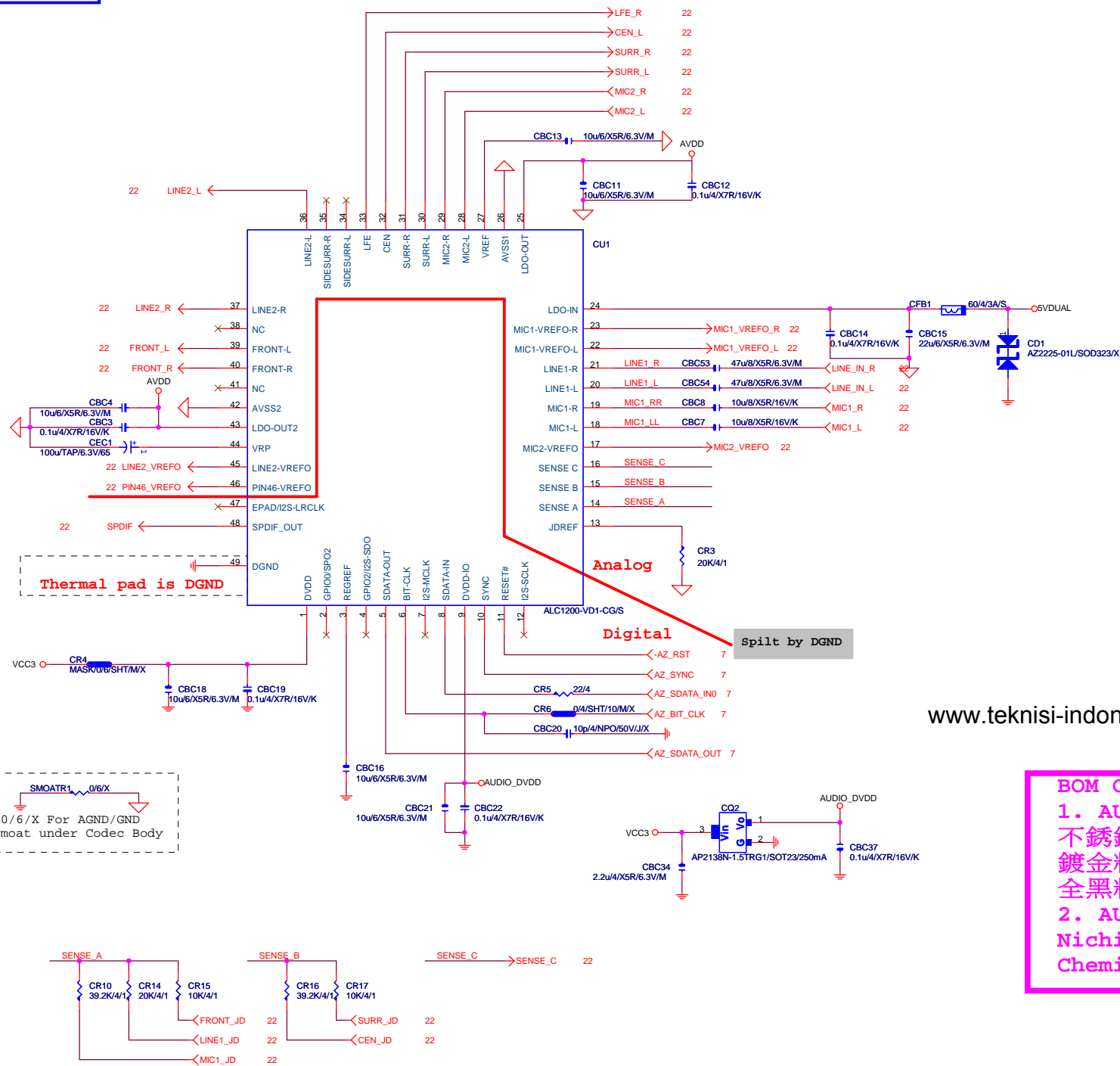
## PWR SHT



## SIO PU



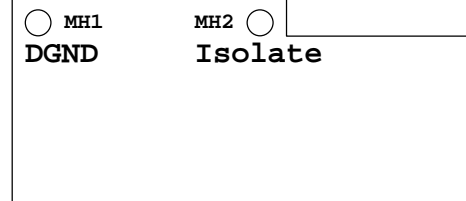




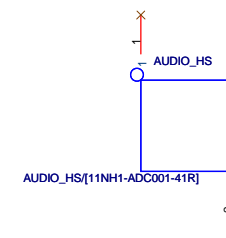
LAYOUT注意:螺絲孔下GND方式

1. MH1下DGND

2. MH2一律改為Isolate

LAYOUT注意:是否要加?  
AGND切割線

音效區域印刷



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BOM OPTION :

1. AUDIO CONNECT

不銹鋼料號:11NR6-403025-A3R

鍍金料號:11NR6-403025-92R

全黑料號:11NR6-403025-B1R

2. AUDIO CAP

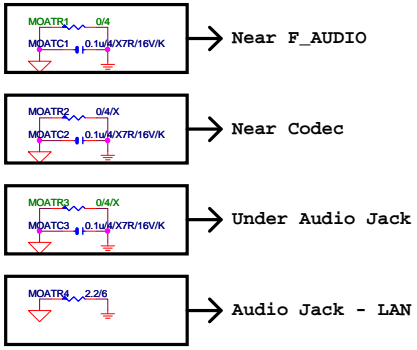
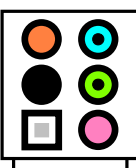
Nichicon MW音效電容 : 100u/TAP/6.3V/65

Chemicon音效電容 : 100uF/TAP/10V/6\*5

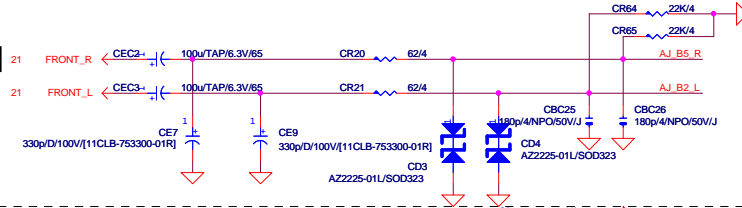
Gigabyte Technology

Title	ALC1220		
Size	Document Number	Rev	
Custom	X570 AORUS ELITE WIFI 1.0		1.0
Date:	Wednesday, June 19, 2019	Sheet	21 of 55

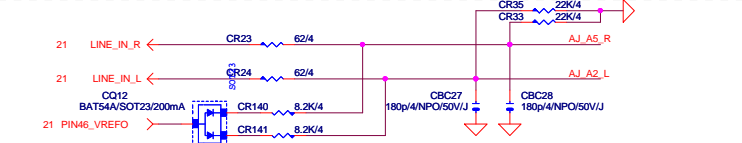
AZALIA JACK



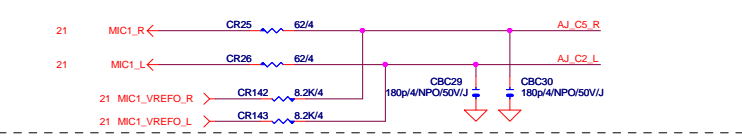
LINE-OUT



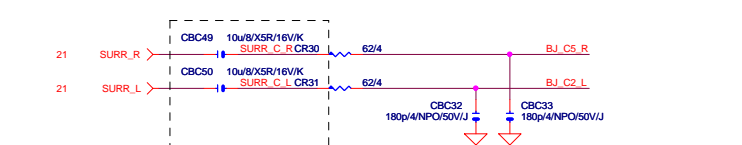
LINE-IN



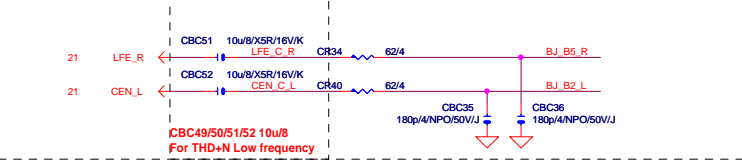
MIC-IN



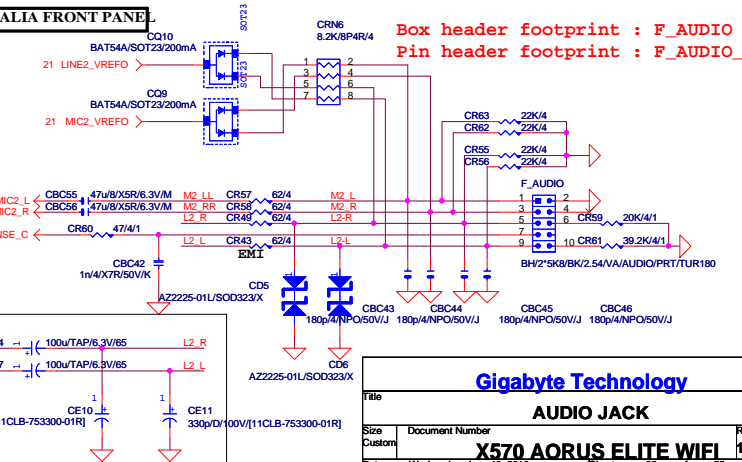
SURROUND



CEN/LFE

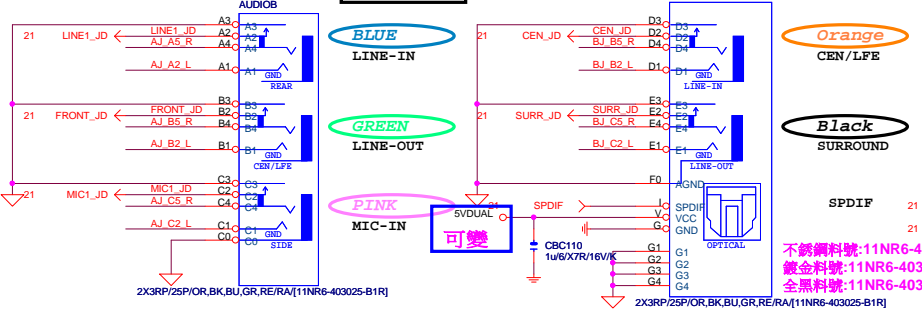


AZALIA FRONT PANE



Box header footprint : F\_AUDIO  
Pin header footprint : F\_AUDIO\_S

AZALIA JACK



Orange  
CEN/LFE

Black  
SURROUND

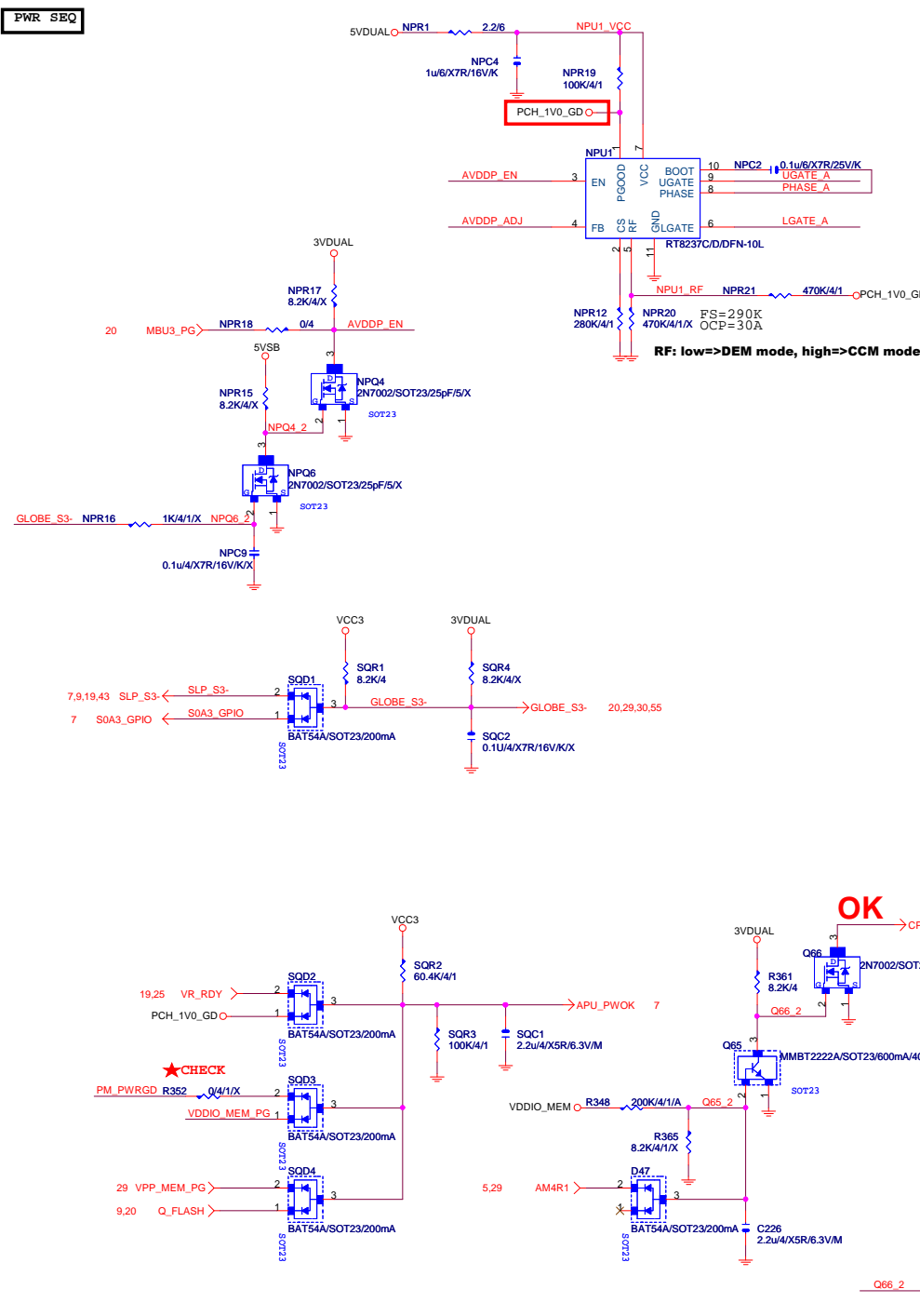
SPDIF

不銹鋼料號:11NR6-403025-A3R  
鍍金料號:11NR6-403025-92R  
全黑料號:11NR6-403025-B1R

Gigabyte Technology

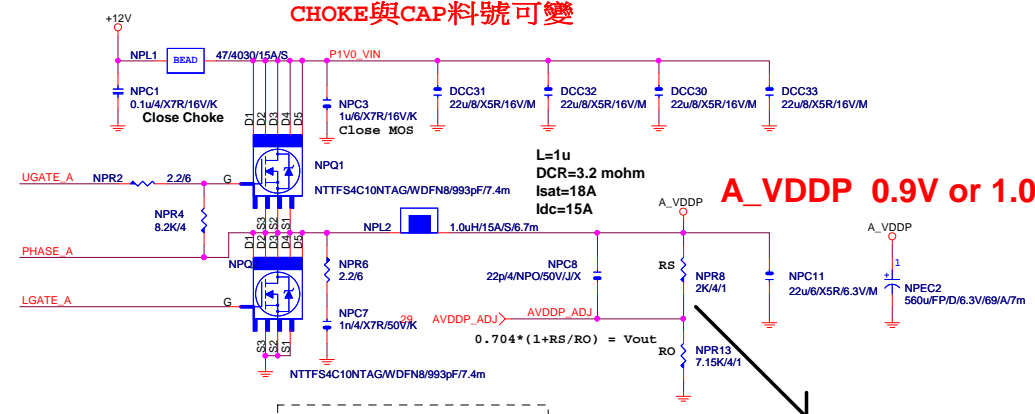
File		
AUDIO JACK		
Size	Document Number	Rev
Custom	X570 AORUS ELITE WIFI	1.0
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RF: low=>DEM mode, high=>CCM mode.

# CHOKE與CAP料號可變



A\_VDDP 0.9V or 1.05V

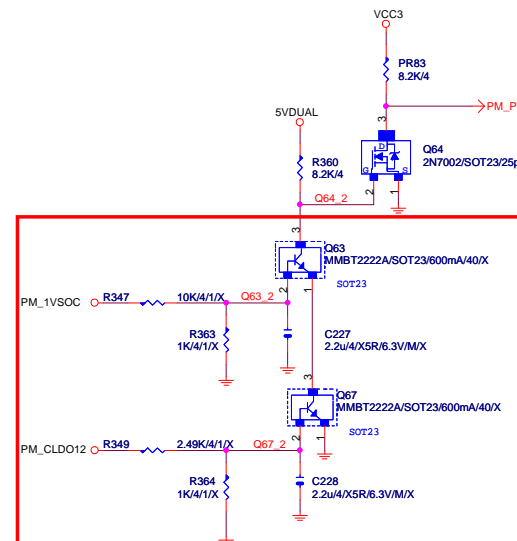
Remote sense請從最重的負載端點拉回



請放置CHOKE一出來的地方

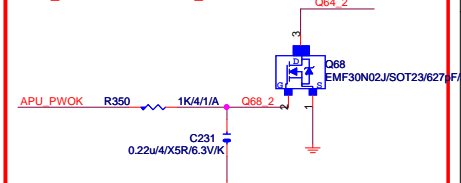
CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

5,7,17,20 CORETYPE1 CORETYPE1 PR85 8.2K/4 NPO7 2



## ★Sequence

APU\_PWOK control PM\_PWGRD

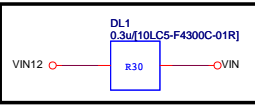
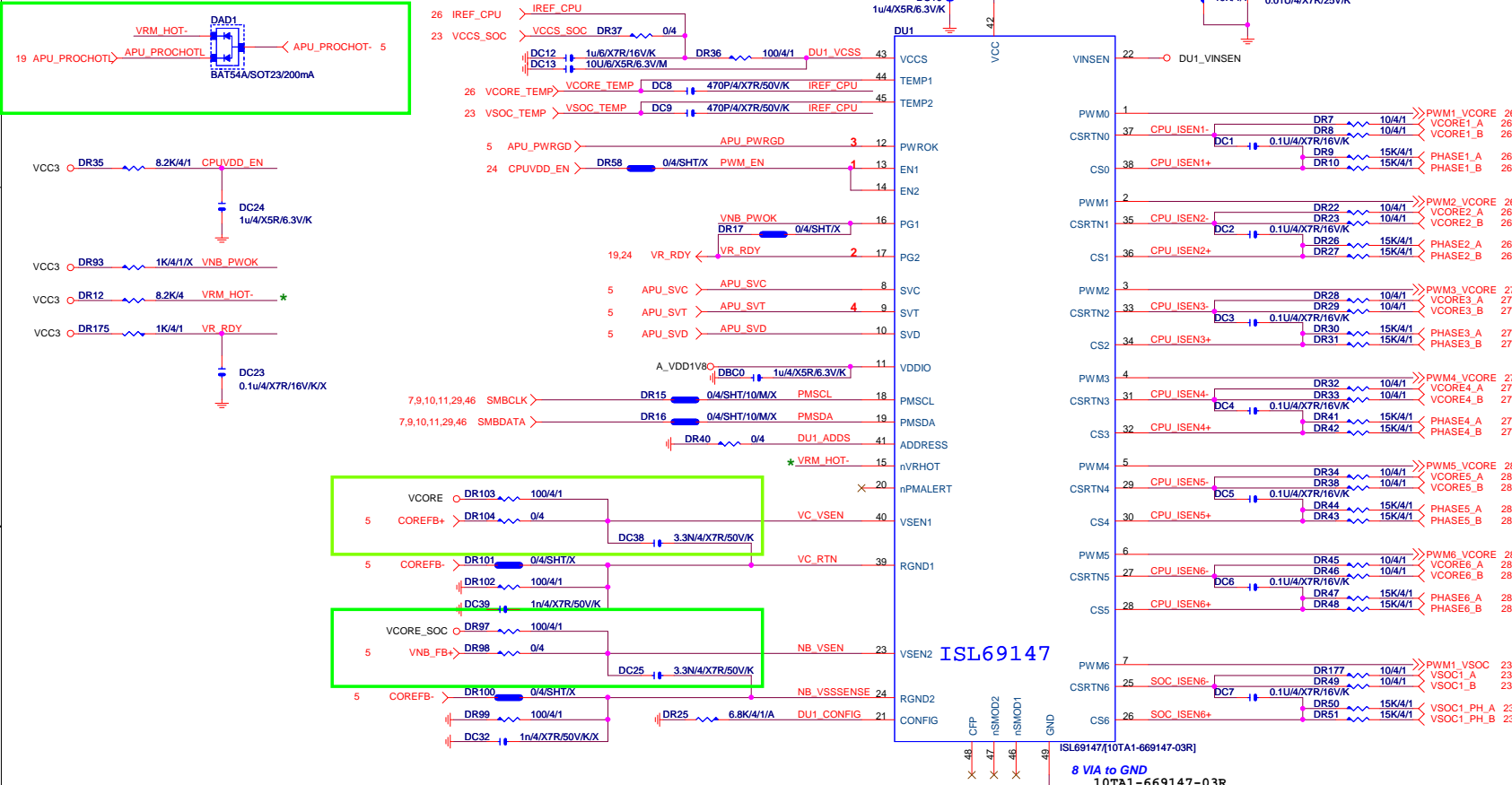


GIGABYTE™

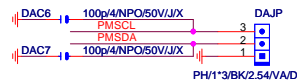
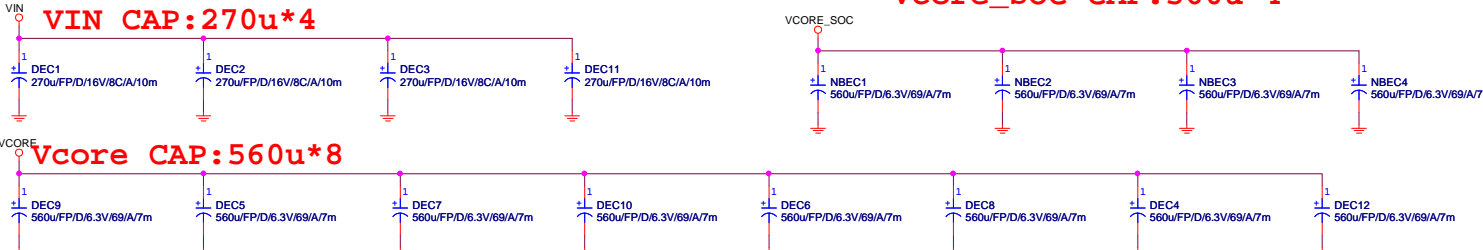
POWER SEQUENCE		
Title	Document Number	Rev
Size	Custom	1.0
Date: Wednesday, June 19, 2019	Sheet 24	of 55



REV:0.1



Vcore SOC CAP:560u\*4

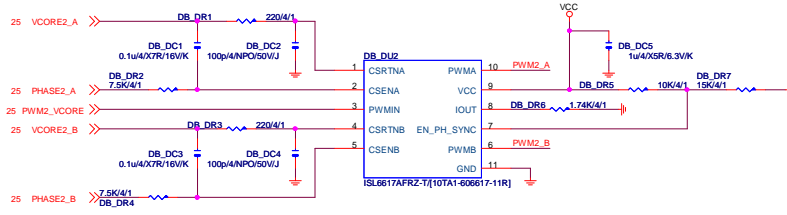
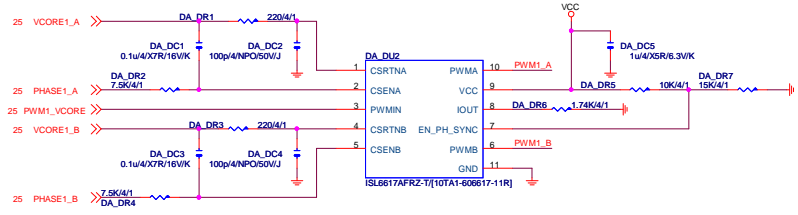
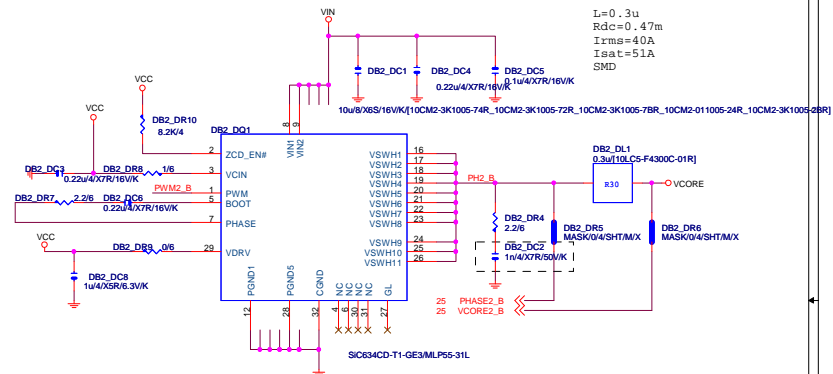
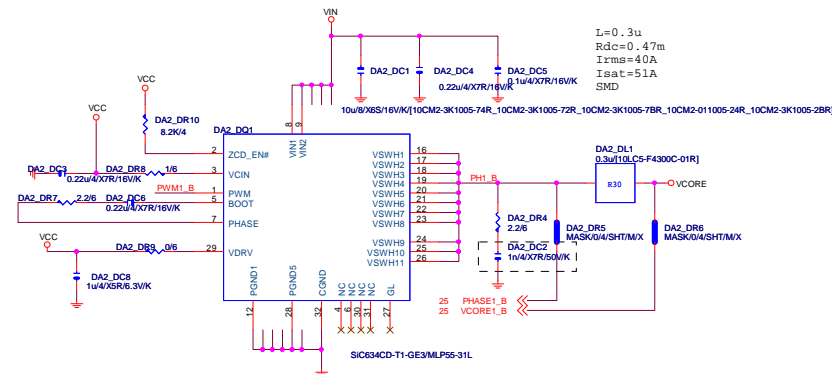
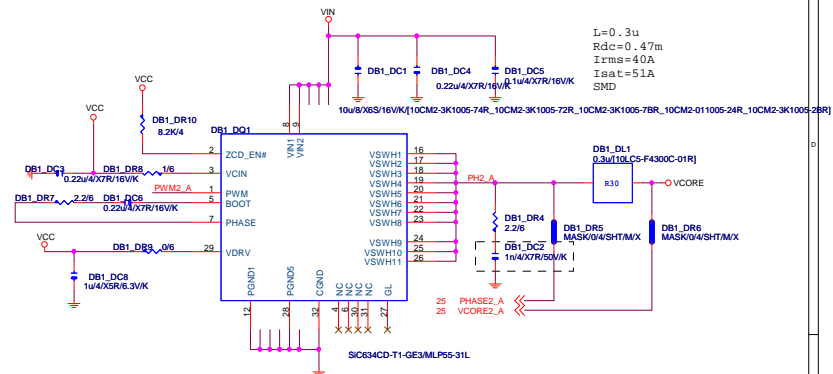
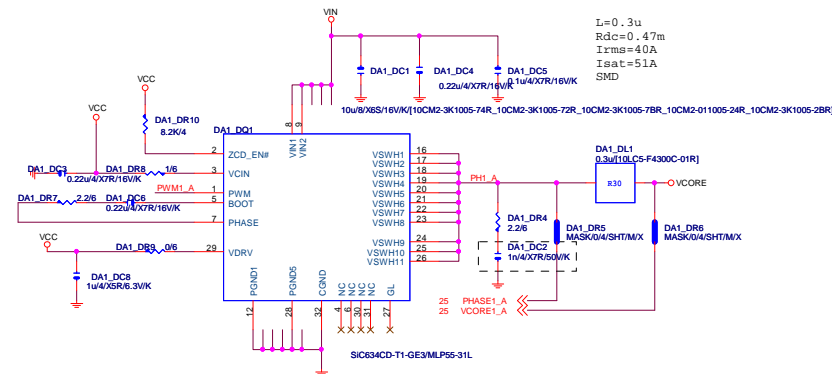


**GIGABYTE**

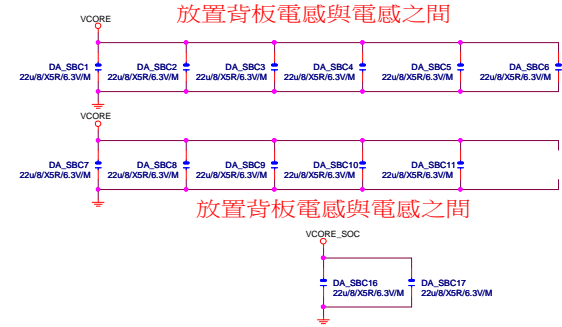
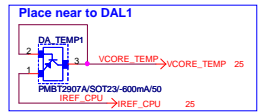
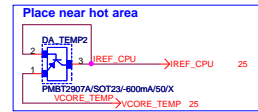
Title	<b>PWM ISL69147</b>
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Size	Document Number
Custom	<b>X570 AORUS ELITE WIFI</b>

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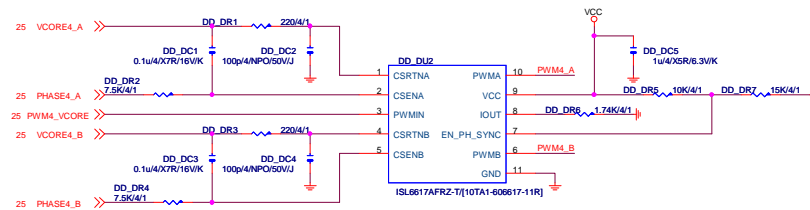
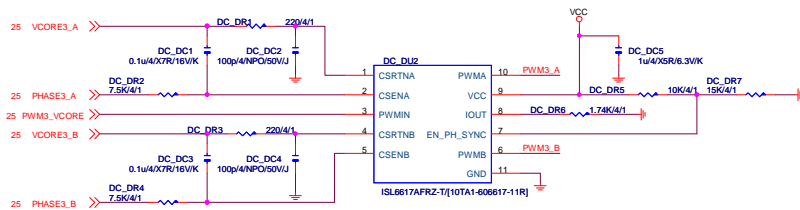
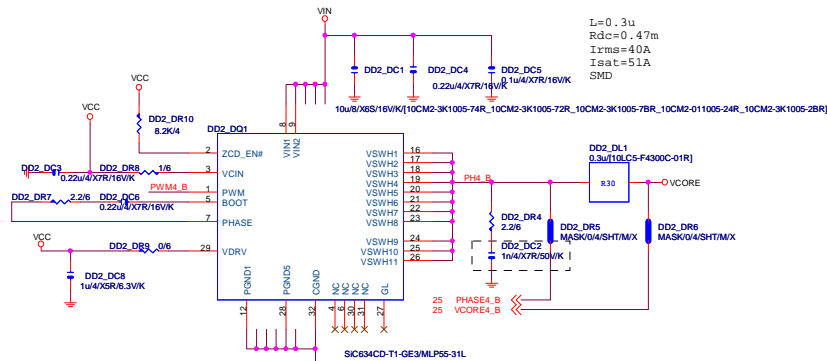
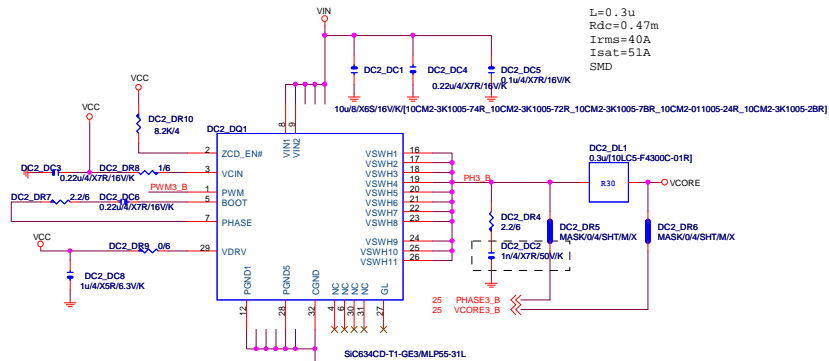
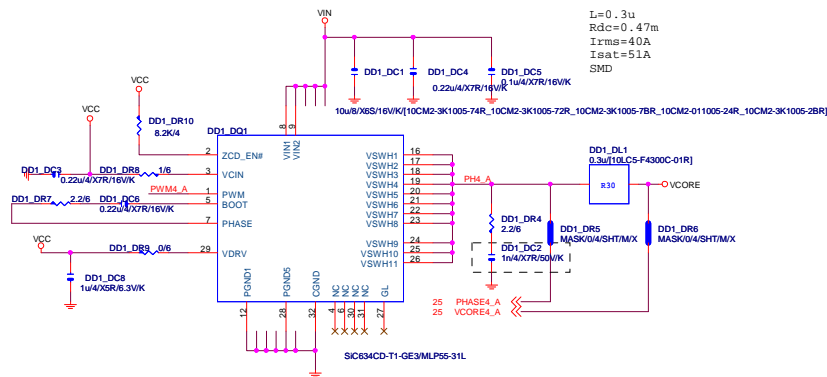
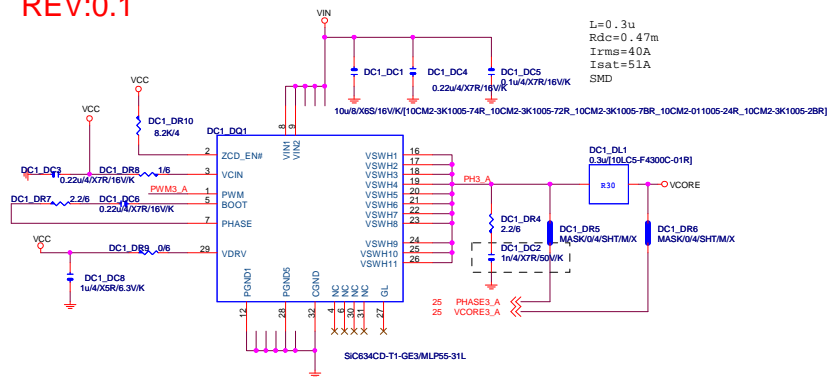


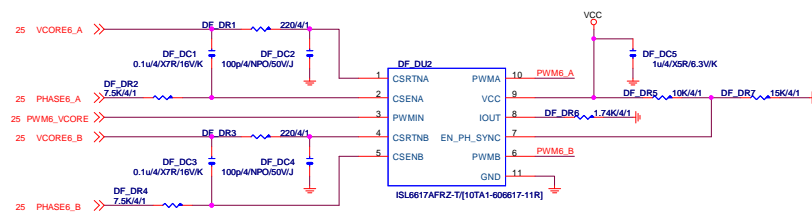
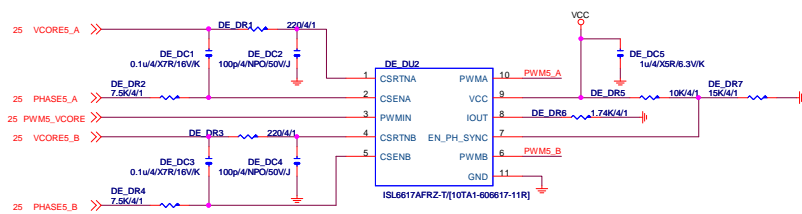
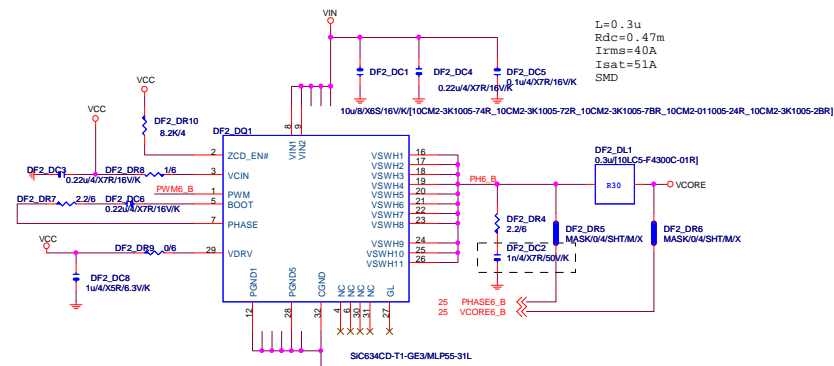
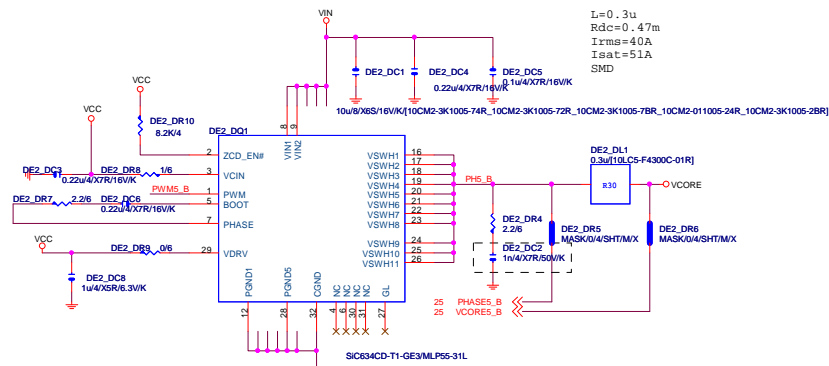
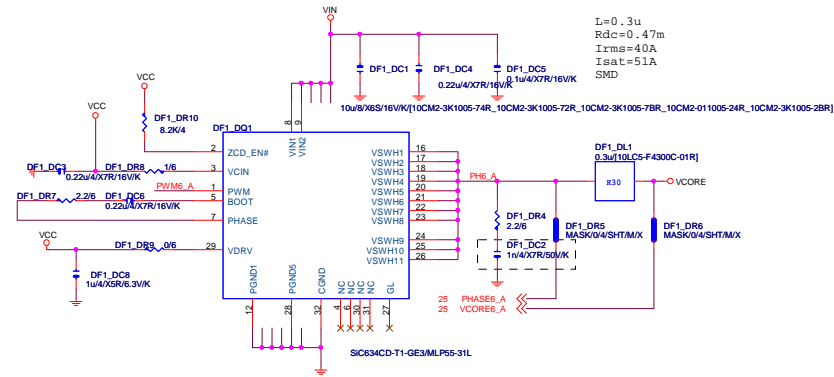
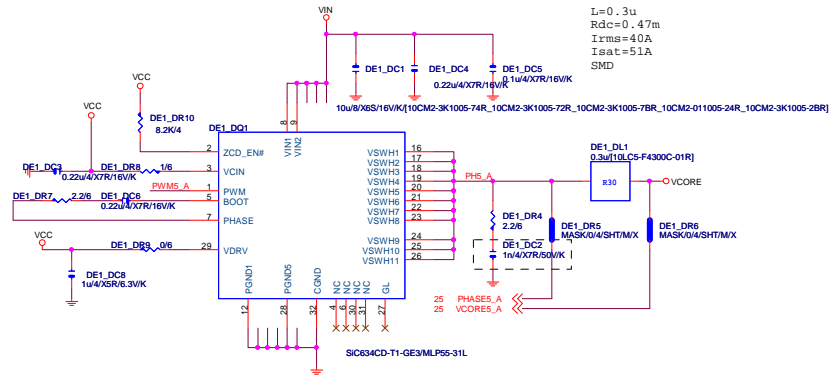
teknisi-indonesia.com



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File	VCORE MOS		
Size	Document Number	X570 AORUS ELITE WIFI	Rev 1.0
Custom			
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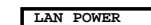
REV:0.1









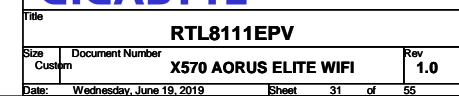
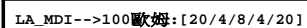


note: lan power連接及電流

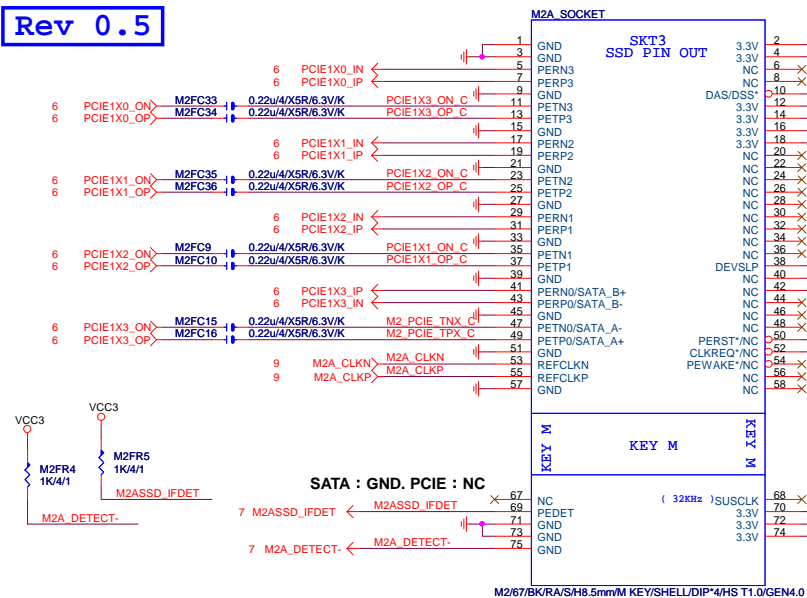


FSVCC\_U3R3 UBR7 150K/4/X -USB0C\_R1 13

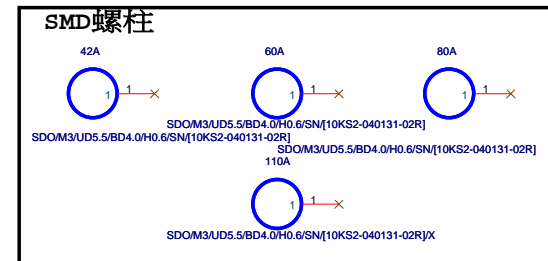
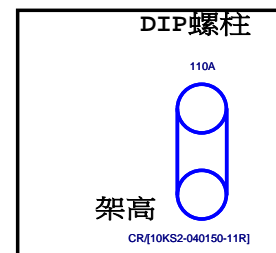
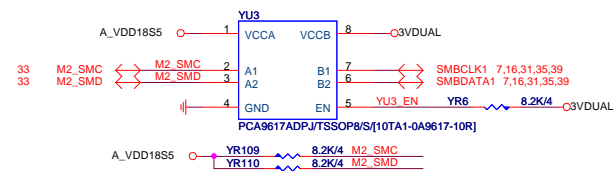
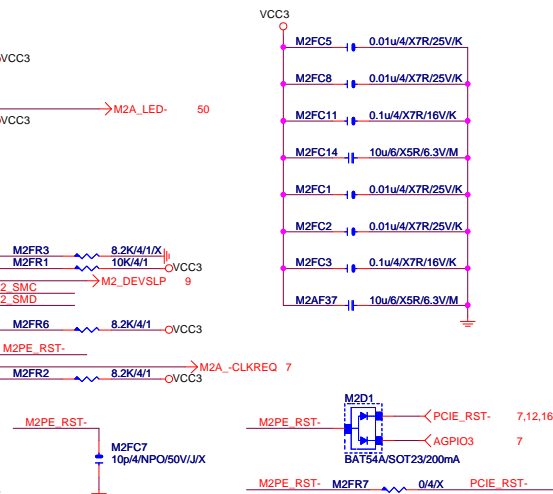
[I210]



Rev 0.5

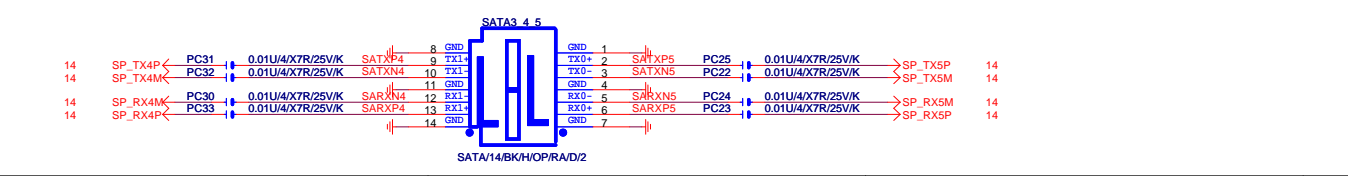
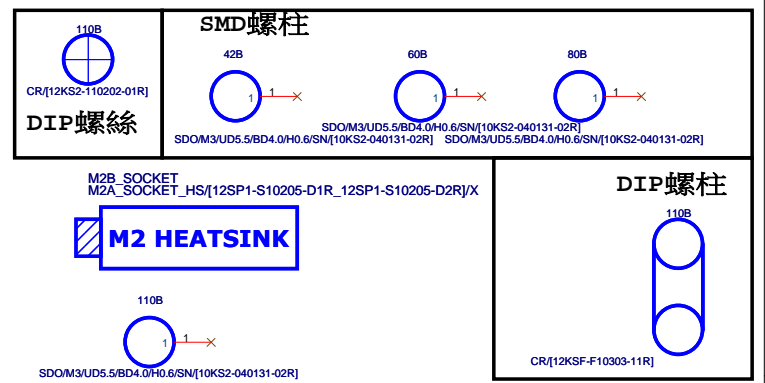
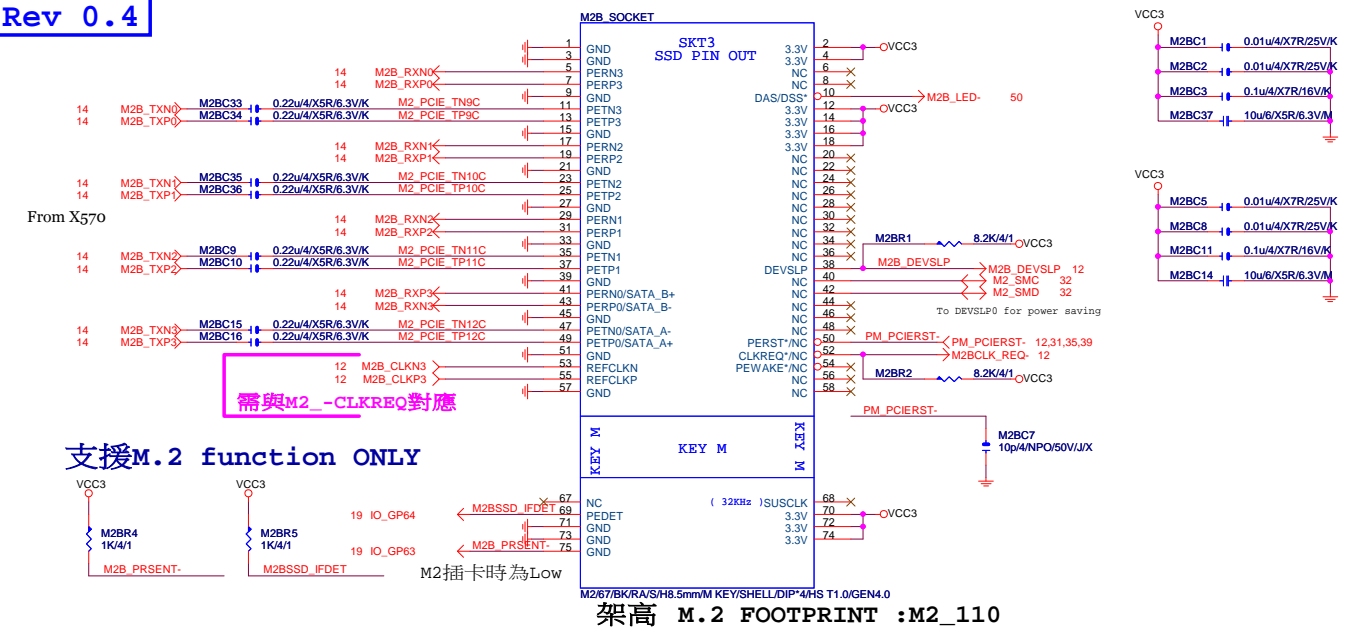


8.5H鐵殼  
Footprint :M2\_110(DIP)



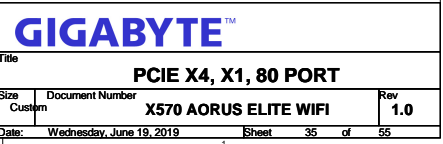
12SP1-S10205-I1R



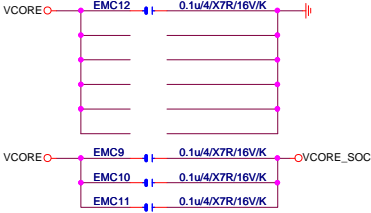
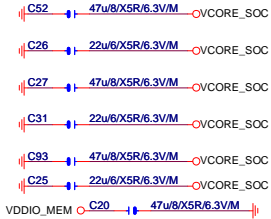
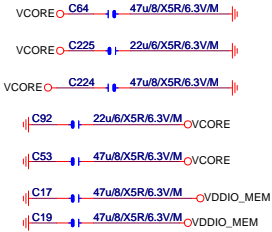
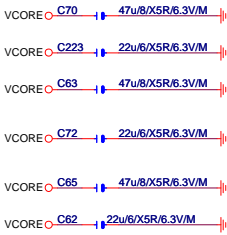


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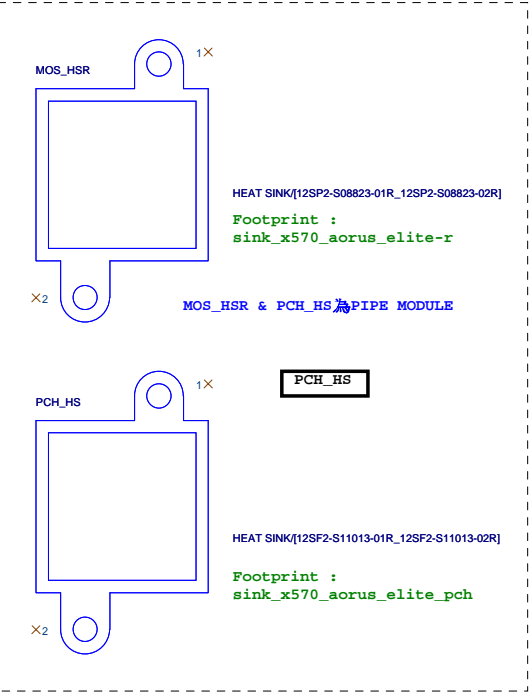
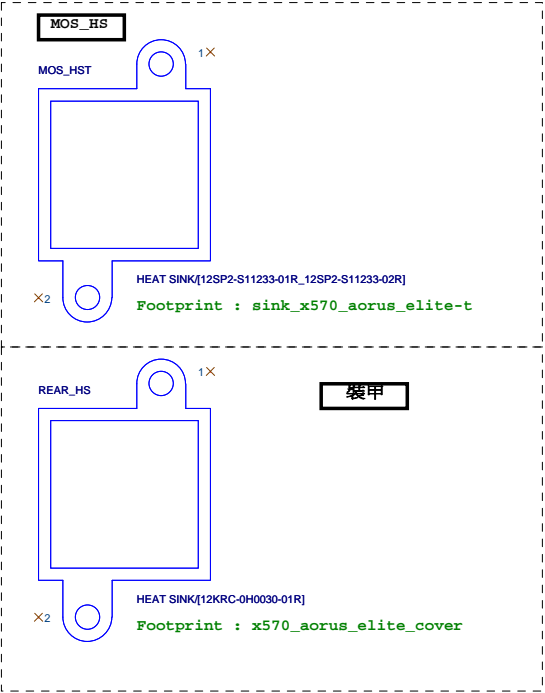
Title			KB_USB_DEC PWR		
Size	Document Number				Rev
Custom	X570 AORUS ELITE WIFI				1.0
Date:	Tuesday, June 18, 2019			Sheet 34 of 55	

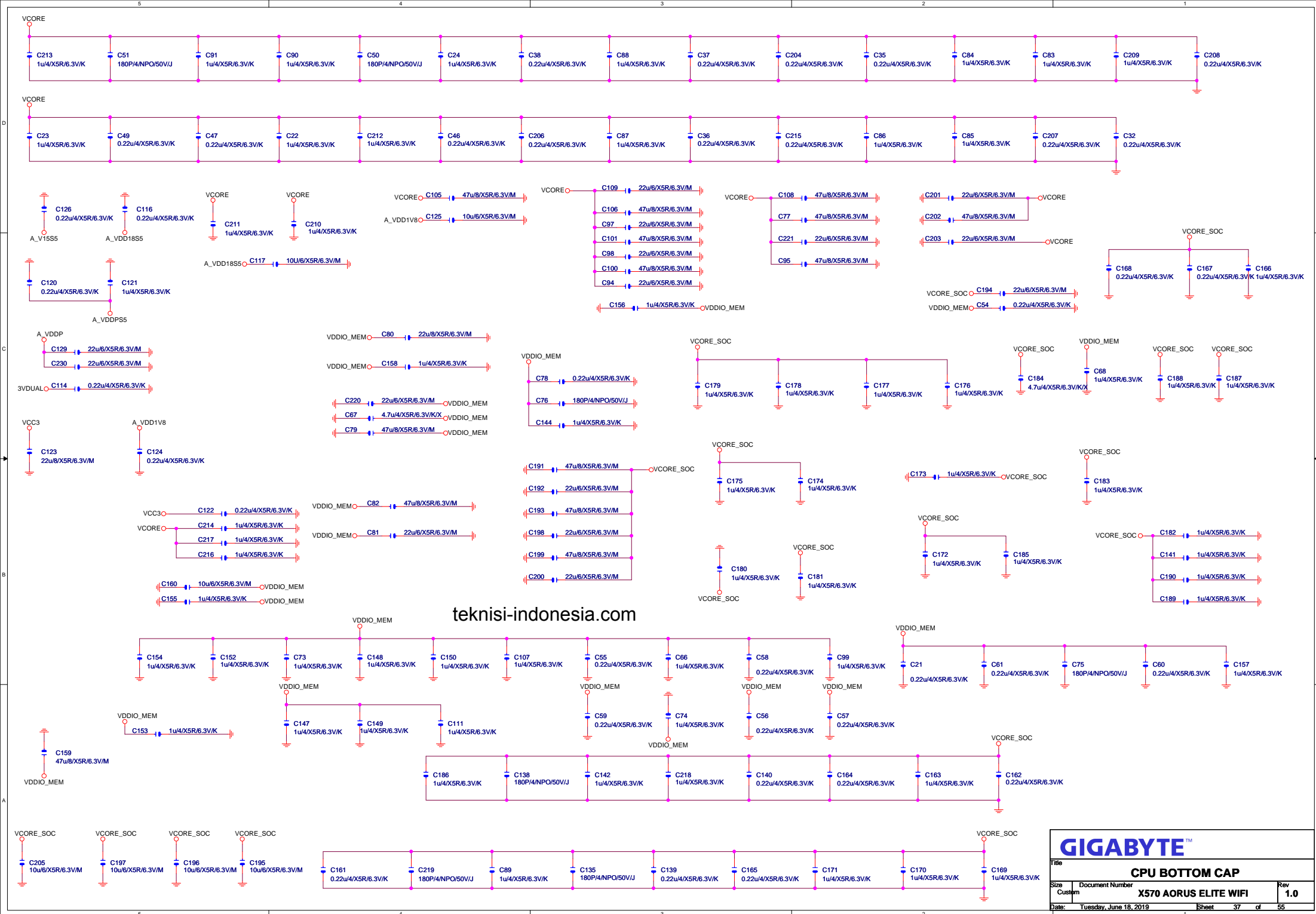


CPU TOP CAVITY



Cross Plane CAP







<b>GIGABYTE</b> <sup>TM</sup>			
Title			
M.2 SOCKET			
Size	Document Number		Rev
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Date:	Tuesday, June 18, 2019	Sheet	38 of 55

The diagram shows the pin connections for the TCU3 component. The pins are numbered 1 through 12. The connections are as follows:

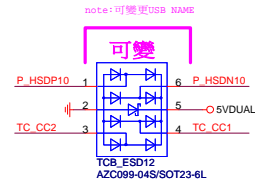
- Pin 1: TC\_CC1
- Pin 2: TC\_CC2
- Pin 3: 321\_CUR
- Pin 4: 321\_PORT
- Pin 5: 321\_VBUS
- Pin 6: 321\_VG\_FAULT
- Pin 7: VCONN\_FAULT#
- Pin 8: VBUS\_DET
- Pin 9: ID
- Pin 10: GND
- Pin 11: DIR
- Pin 12: VDD

External components and connections include:

- TCR1 (10K/4/1) connected to Pin 1 and 5VDUAL.
- TCR10 (4.7K/4) connected to Pin 2 and 5VDUAL.
- TCR4 (8.2K/4) connected to Pin 6 and 5VDUAL.
- 3212\_EN connected to Pin 9 and TCR25 (1K/4/1) connected to Pin 12.
- 3212\_EN is also connected to Pin 10.
- 3212\_EN is also connected to Pin 11.
- 3212\_EN is also connected to Pin 12.
- 3212\_EN is also connected to Pin 10.
- 3212\_EN is also connected to Pin 11.
- 3212\_EN is also connected to Pin 12.
- 3212\_EN is also connected to Pin 10.
- 3212\_EN is also connected to Pin 11.
- 3212\_EN is also connected to Pin 12.
- 3212\_EN is also connected to Pin 10.
- 3212\_EN is also connected to Pin 11.
- 3212\_EN is also connected to Pin 12.

The component is identified as TUSB321RWBR/0FN12/S[10H05-600321-00R].

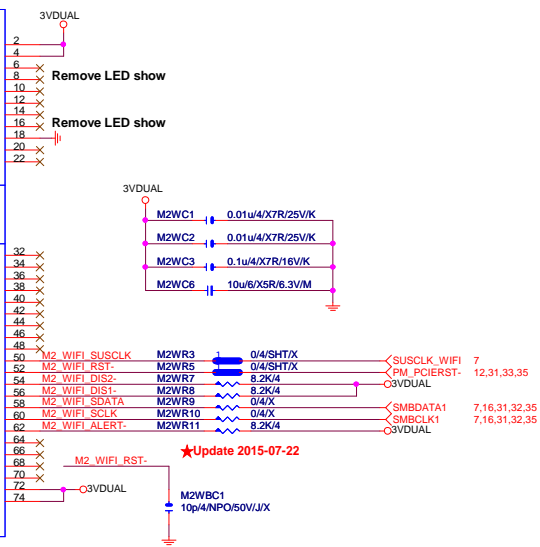
L - Default current / Pull down to GND or NC  
M - Medium (1.5A) current / Pull up to VDD 500K  
H - High (3.0A) current / Pull up to VDD 10K



H - HOST  
L - Device  
NC - Dual Role



PCIE:15/4/4/15(breakout min 8/4/4/4/8)  
內層 Impedance=85 +- 12%



★Update 2015-07-22  
★Footprint for  
直立式 SMD:  
WIFI-EKEY

★Footprint for 横躺式SMD:  
NO55-F-35D-2

一套WIFI MODULE包含外框+WIFI CARD+天線



<b>M.2, F_TYPE C</b>					
Size Custom	Document Number <b>X570 AORUS ELITE WIFI</b>				Rev <b>1.0</b>
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<b>GIGABYTE™</b>			
Title <b>M.2 SOCKET</b>			
Size Custom	Document Number <b>X570 AORUS ELITE WIFI</b>		Rev <b>1.0</b>
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5	4	3	2	1
D				
C				
B				
A				
5	4	3	2	1

<

<b>GIGABYTE™</b>			
Title <b>M.2 SOCKET</b>			
Size Custom	Document Number <b>X570 AORUS ELITE WIFI</b>		Rev <b>1.0</b>
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5	4	3	2	1
D				D
C				C
B				B
A				A

<b>GIGABYTE™</b>		
Title		
<b>PCIE X8, SWITCH</b>		
Size	Document Number	Rev
Custom	<b>X570 AORUS ELITE WIFI</b>	<b>1.0</b>
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5	4	3	2	1
D				D
C				C
B				B
A				A

<b>GIGABYTE™</b>			
Title <b>DIGITAL LED</b>			
Size Custom	Document Number <b>X570 AORUS ELITE WIFI</b>		Rev <b>1.0</b>
Date: <b>Tuesday, June 18, 2019</b>	Sheet <b>44</b>	of <b>55</b>	

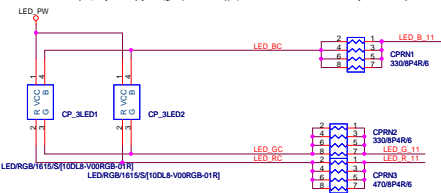
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**GIGABYTE™**

Title			
ASM 2142 U31			
Size	Document Number		Rev
Custom	X570 AORUS ELITE WIFI		1.0
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## 第一區 LED

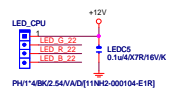
FOR 裝甲高亮度 正發光 LED\*2 (位置在正板,依據裝甲設計擺放)



FOOTPRINT: LED\_4P\_RGB高亮度

## 第二區 LED

燈條 LED (LED\_CPU放在CPU附近位置)

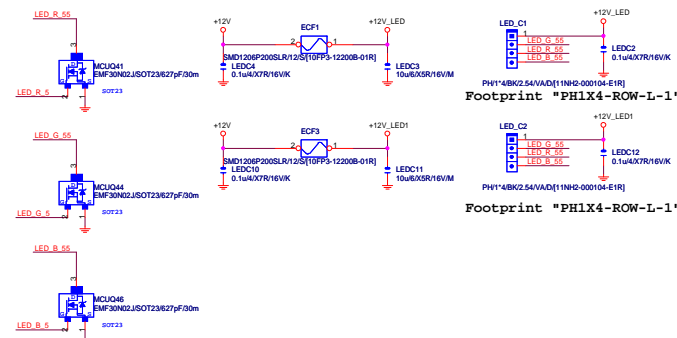


Footprint "PH1X4-FAN-AMD-L"

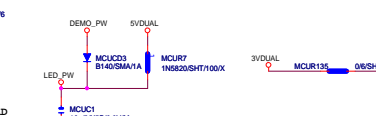
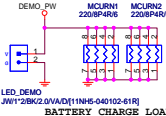
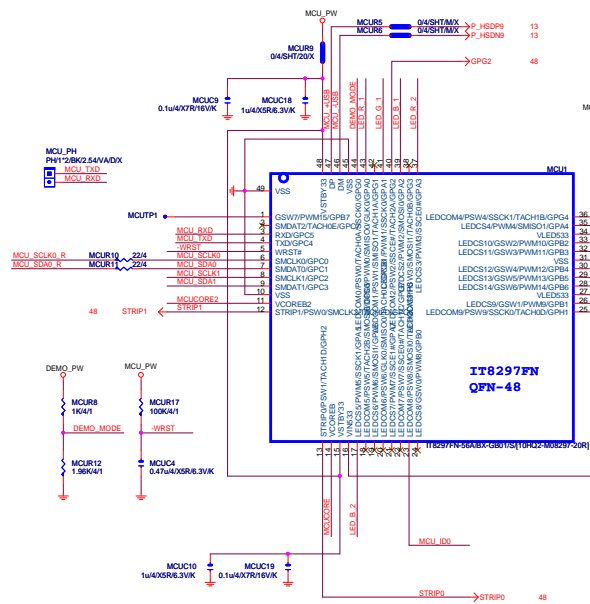
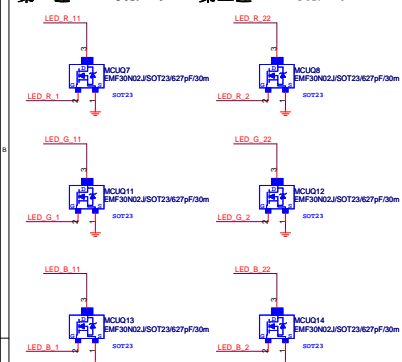
## 第五區 LED

燈條 LED (LED\_C1放在PCB左邊板邊位置)

燈條 LED (LED\_C2放在PCB右邊板邊位置)



## 第一區 LED CONTROL 第二區 LED CONTROL



For AMD MCU update

SEL	Y+	Y-
L	M+	M-
H	D+	D-

Default SMBUS

SMBUS

SMBUS

SMBUS

SMBUS

SMBUS

SMBUS

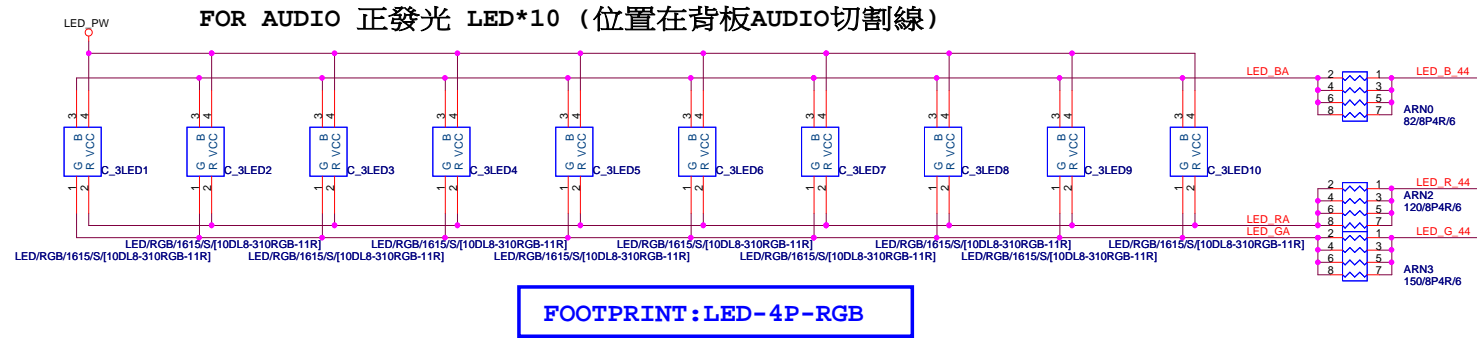
SMBUS

SMBUS

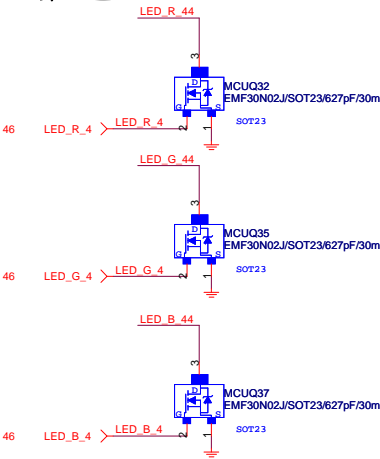
GIGABYTE

第三區 LED

第四區 LED



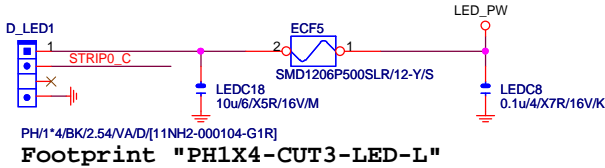
第四區 LED CONTROL



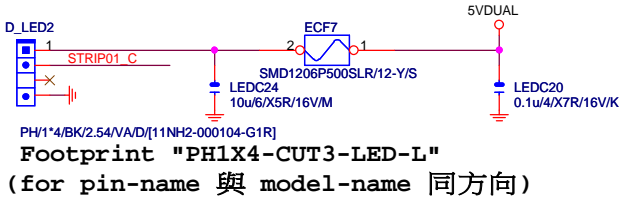
第六區 LED (靠近左上板邊位置)

(靠近右下CPU板邊位置)

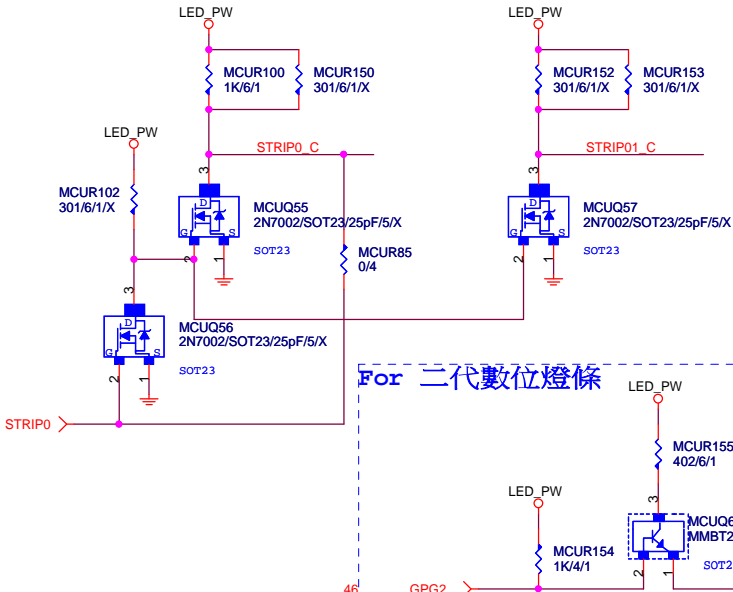
Digital LED Strip1



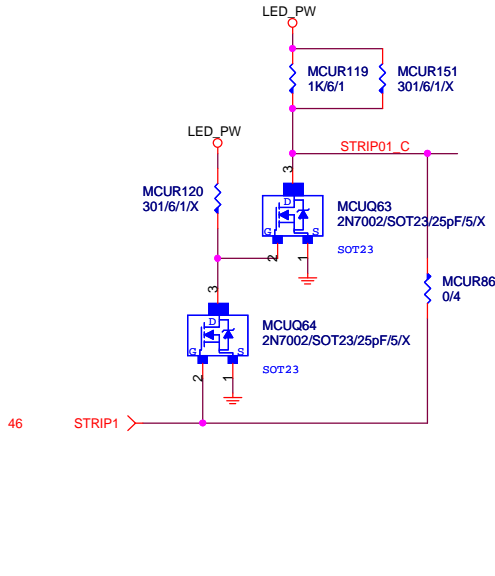
Digital LED Strip2



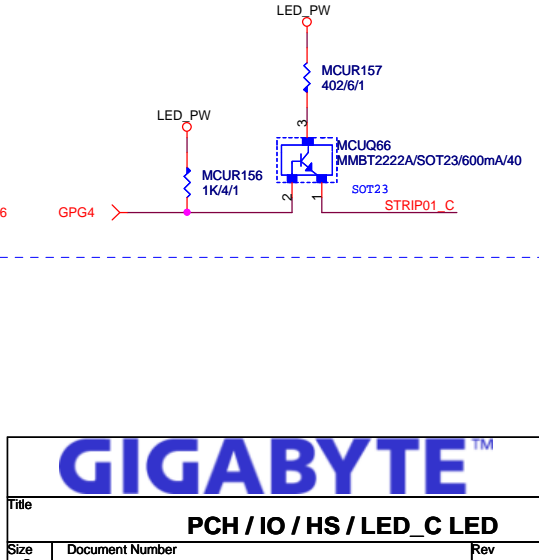
燈條 Level shift



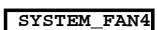
燈條 Level shift



For 二代數位燈條

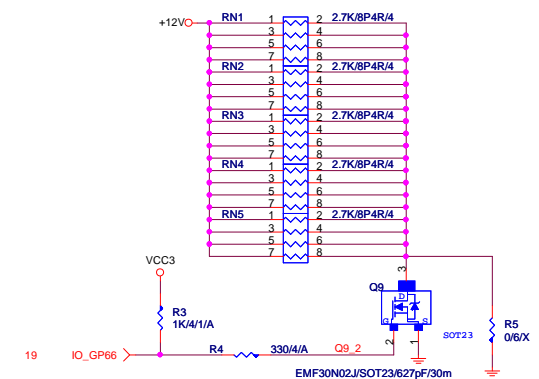
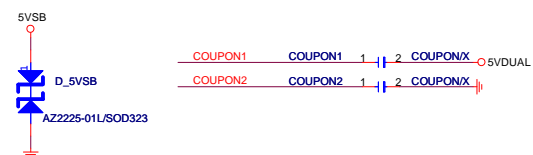
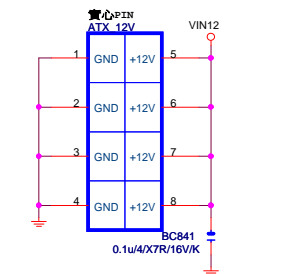
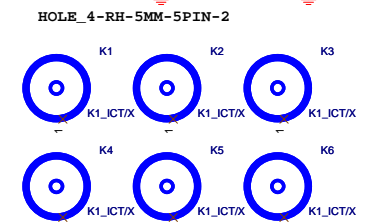
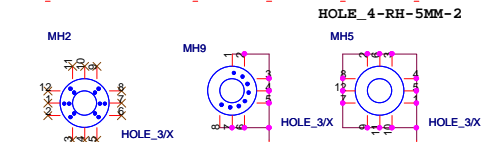
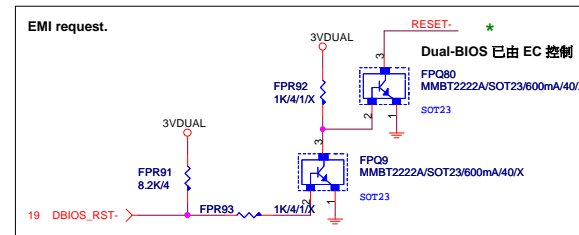
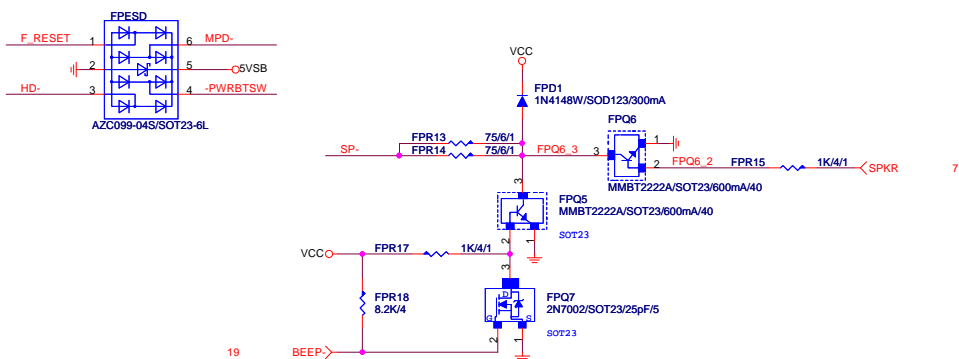


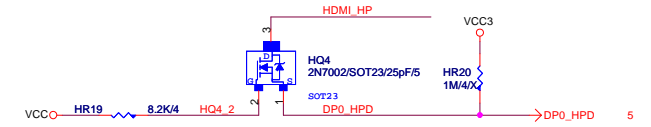
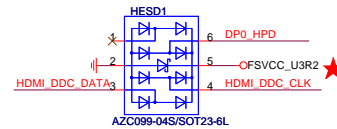
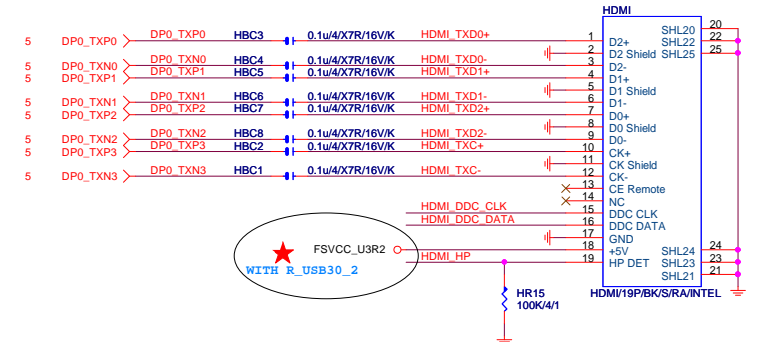
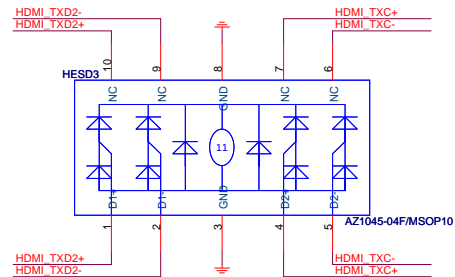
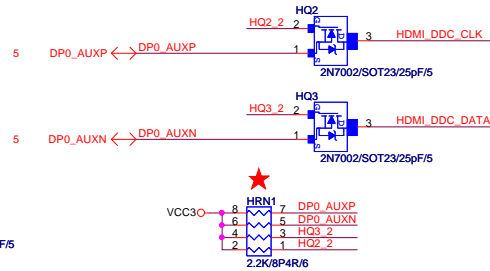




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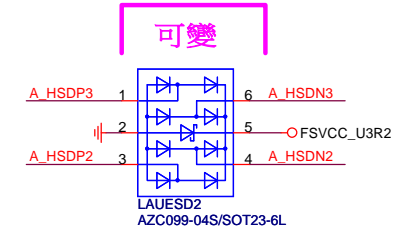
Title			
PCIE X8, SWITCH			
Size	Document Number		Rev
Custom	X570 AORUS ELITE WIFI		1.0
Date:	Wednesday, June 19, 2019	Sheet	49 of 55



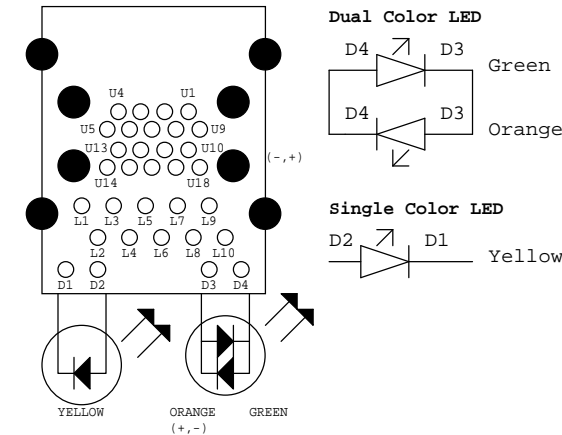


USB\_LAN CONNECTOR R1.0

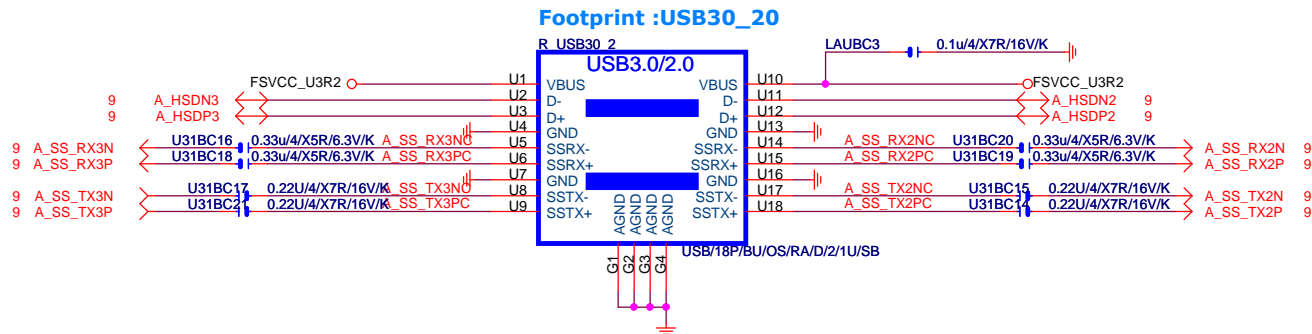
RMA ESD PROTECT note:可變更USB\_NAME



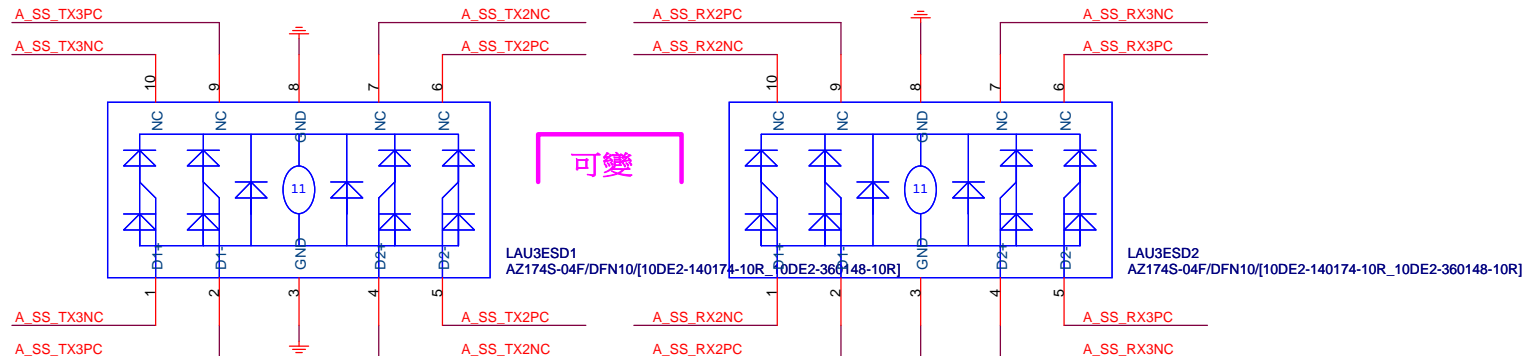
USB30\_LAN LAYOUT示意图



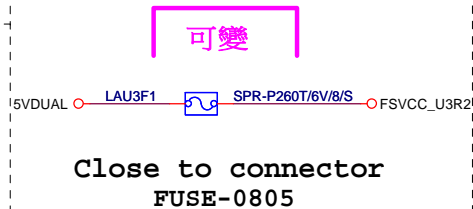
USB\_LAN CONNECTOR note:可變更USB\_NAME



RMA ESD PROTECT note:可變更USB\_NAME



USB POWER note:可變更FUSE



EMI SHORT PAD PS:視EMI需求

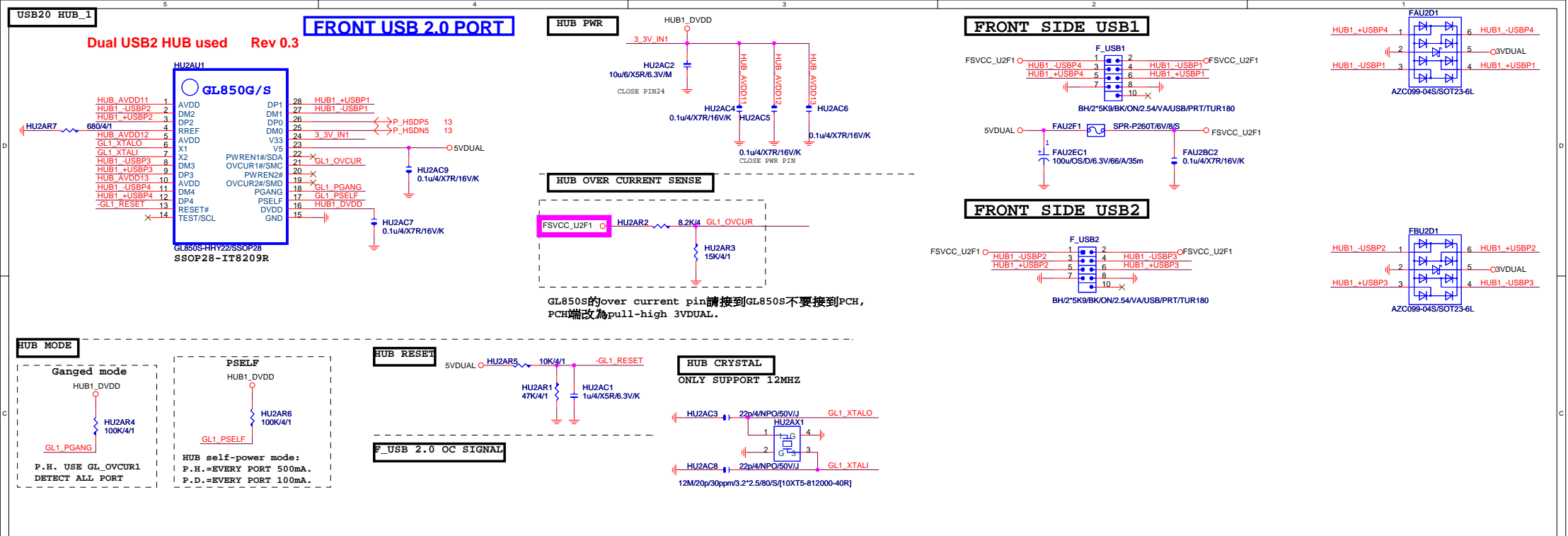
LAN POWER note: lan power連接及電流

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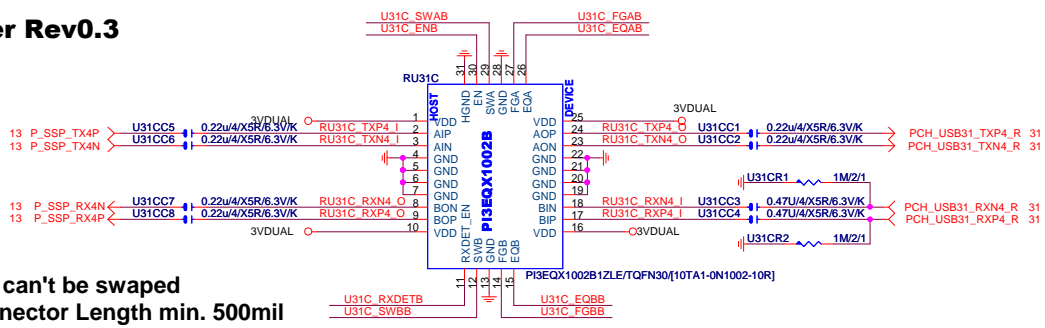
Title  
**Realtek RTL8125**

Size Custom	Document Number <b>X570 AORUS ELITE WIFI</b>	Rev <b>1.0</b>
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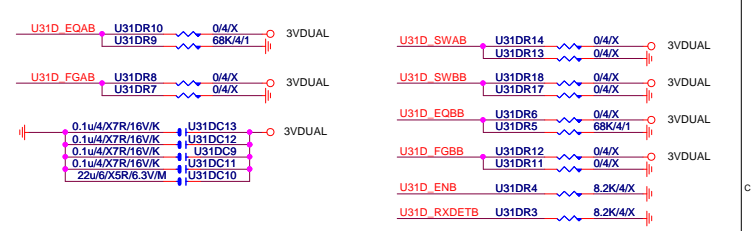
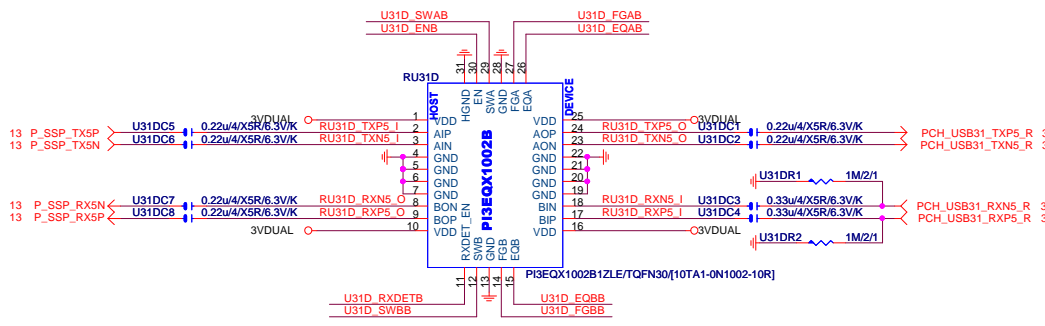
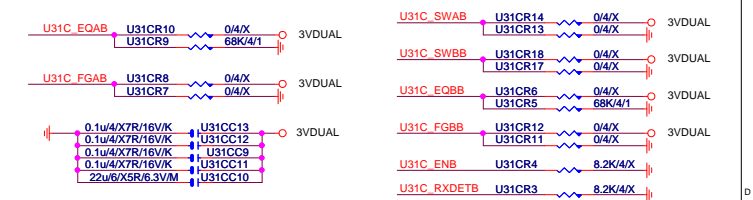
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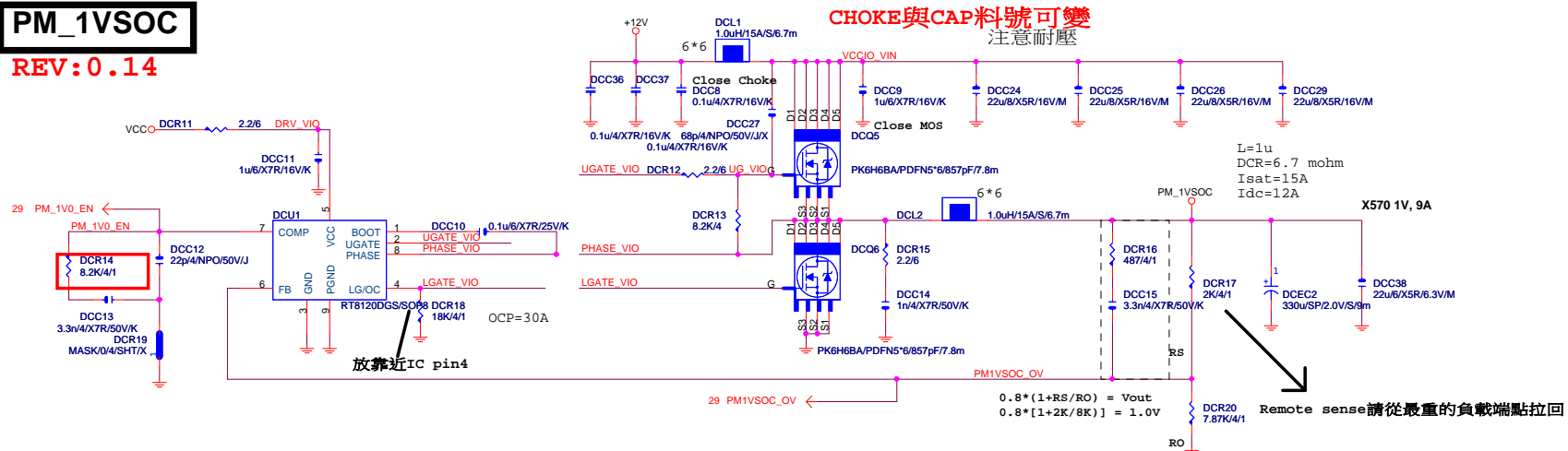
TypeA Redriver Rev0.3



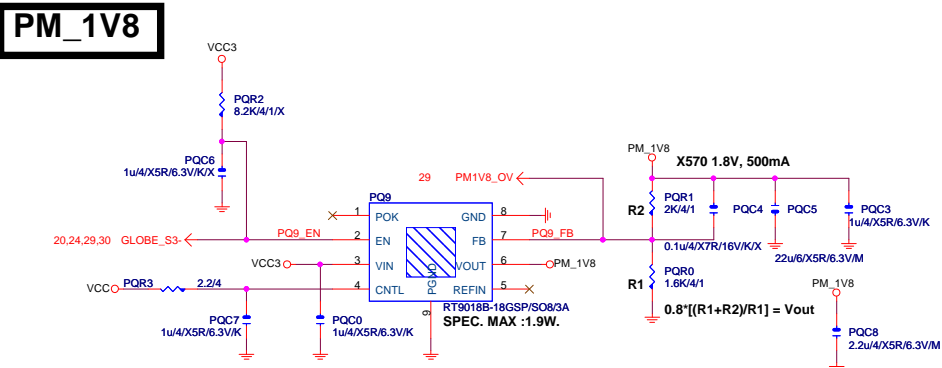
Layout Rule:  
1. Differential Pair can't be swaped  
2. Redriver to Connector Length min. 500mil



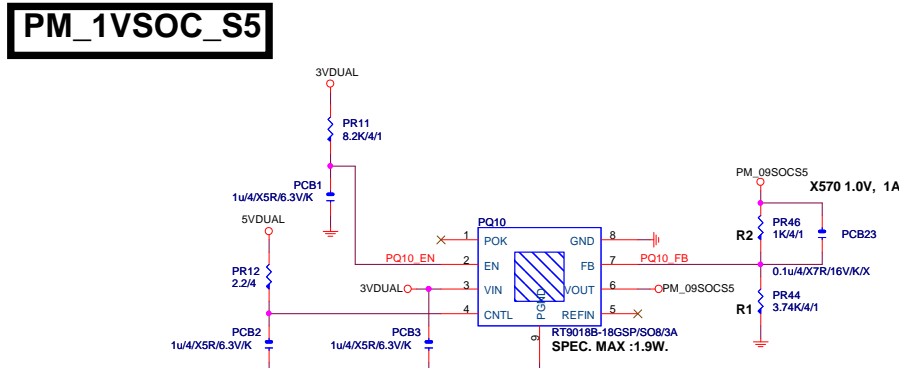
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PM\_1V8

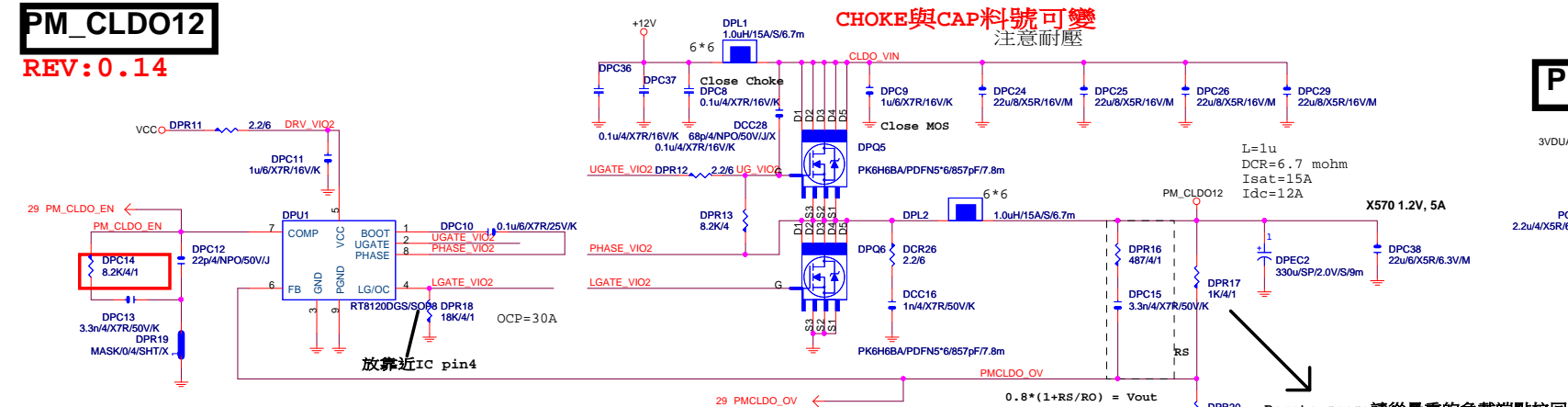


PM\_1VSOC\_S5

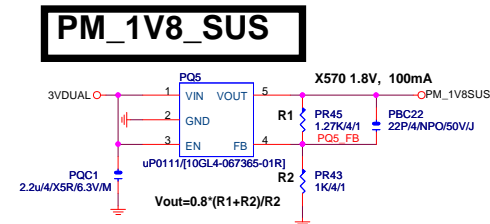


PM\_CLDO12

REV:0.14



PM\_1V8\_SUS



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							<b>1.0</b>
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